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APIC Input Port

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1 Overview

The InputPort interface to the outside world is UTOPIA compliant for both 8 and 16 bit datapaths. Below is the external view of the InputPort component. The top right group of signals are the interface to the InputSynch which synchronizes data and control signals coming/going to the internal clock domain. At the bottom right is the gfcclav pin which sends the value of gfc(0) for each incoming cell to a linked OutputPort for GFC based flow control. On the top right side is the external interface to the OutputPort. At the top are the pins making up the UTOPIA port, below that is a group of miscellaneous external signals including clock, reset, strap signals, and an output signal rxgrant. Rxgrant is used for explicit pin based flow control to APICs connected via PCB traces or a ribbon cable. More details on both pin based and GFC based flow control can be found in : **technoteflow control**.

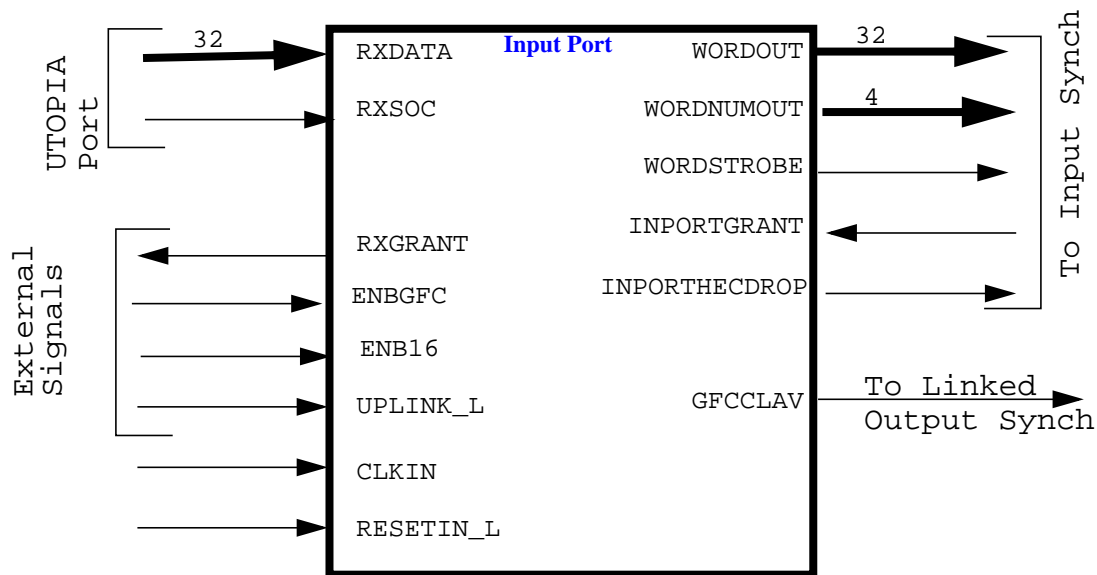


Figure 1: Input Port External Block Diagram

1.1 External Input Interface

Below is a list of the external pins with direction and short description of funtion.

Table 2: Rx External Signals

Name	Direction	Function
RXDATA	I	8/16 bit data path
RXSOC	I	Start Of Cell - asserted on first word of cell
RXGRANT	O	Flow control signal for direct-connect to other APICs
ENB16	I	Enable 16 bit mode
ENBGFC	I	Enable GFC flow control bit mode
UPLINK_L	I	Indicates whether the link is up

The InputPort can be viewed as two separate state machines. The first machine handles data movement and the second machine generates control signals.



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The data movement machine watches RXSOC and takes data in on the RXDATA port.. This machine assumes that entire cells will appear as contiguous words on RXDATA immediately following the RXSOC signal. No cell is ever dropped in the InputPort. Instead, cells will be dropped by the VCXT if the CellStore is too full to accept them. Note that if RXSOC is asserted before a cell has been transmitted to the APIC, the interrupted cell and the first new cell are lost, but then the InputPort resumes normal operation with the RXSOC pattern.

Flow control in the APIC is handled in a few different ways. When the APIC is attached to a UTOPIA PHY device, flow control is strictly between the PHY and the APIC and is handled by the control signal state machine. When the APIC is attached to another APIC via board traces or ribbon cable, the RXGRANT signal (from the CellStore's flow control threshold) is used as TXCLAV on the transmit interface. The flow control unassigned cells are discarded in the InputPort. Regardless of the mode of the InputPort, the GFCCLAV signal contains the value of GFC[0] from the last cell received by the InputPort. This signal is fed to the transit OutputPort after passign through the OutputSynch, and can be used for flow control if the OutputPort's ENBGFC pin is set. For more details on APIC flow control see **technoteflowcontrol** .

UPLINK_L indicates that a link has been established for both the GLink and SONET. When the connection to another ATM device is via printed circuit board trace or ribbon cable, the UPLINK_L signal is tied active low on the PCB. This signal must be active for the InputPort to indicate that is has valid data to the VCXT.

