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Output Port Design

Version 1.0
August 12, 1998

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1 Overview

The Output Port is a submodule of the APIC with a external UTOPIA interface both 8 and 16 bit wide datapaths. Below is the external view of the output port component. The top left group of signals are the interface to the internal submodule called the OutputSynch which synchronizes data and control signals coming from other clock domains. At the bottom left are the clock and reset signals. On the right side is the external interface. Below the external signals are the strap signals which will be pulled high or low on the PCB. The pins enbgfc, generategfc, and gfcclav are related to the proprietary APIC flow control documented in: **Tech Note Flow Control control.**

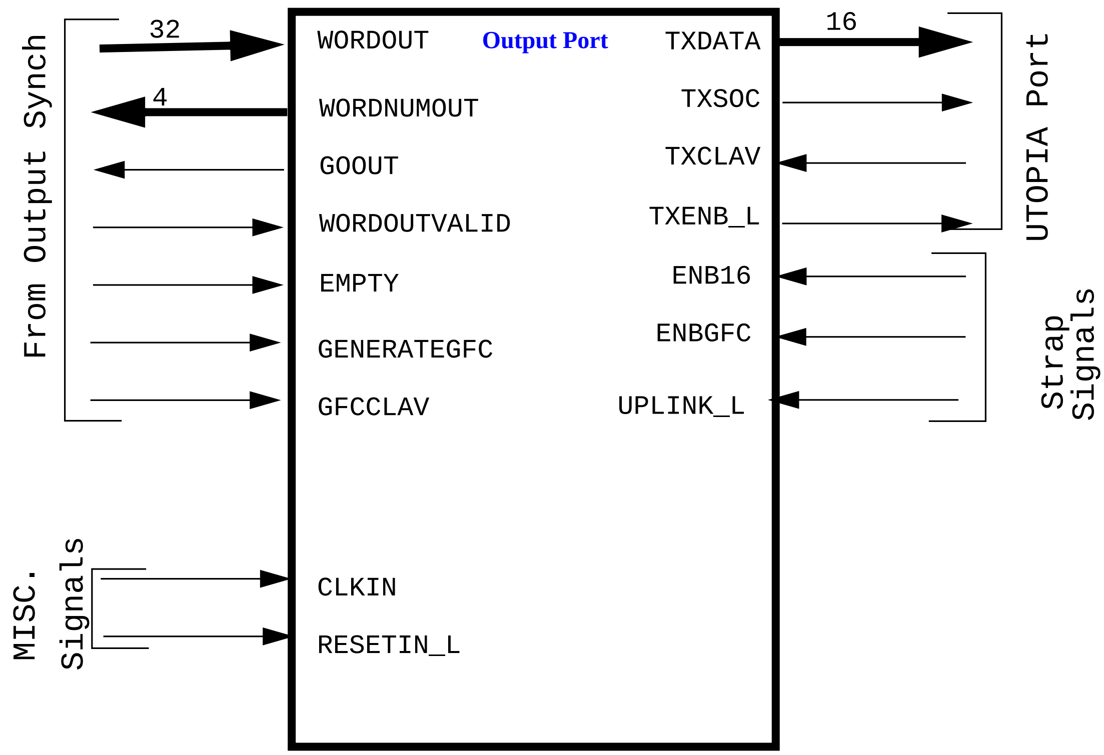

Figure 1: External Block Diagram of Output Port

2 OutputPort Interfaces

2.1 External Interface

The Table below gives the name,direction, and function of each of the external pins (on the top right side of the above figure).

Name	Direction	Function
TXDATA	O	8/16 bit data path
TXSOC	O	Start Of Cell - asserted on first word of cell
TXENB_	O	FIFO write signal for PHY devices (active low)

Name	Direction	Function
TXCLAV	I	Cell Slot Available on PHY device (possibly out of phase with clock due to long delay over ribbon cable - synchronize it!)
ENB16	I	Enable 16 bit mode
ENBGFC	I	Use GFC flow control method (and TXCLAV)
UPLINK_L	I	Not used in the Output Port any more.

An important issue with the UTOPIA port design has to do with the specification relating to when TXCLAV can assert in relation to the start of cell. The picture below shows the APIC's UTOPIA port for the 16-bit case without using GFC flow control. Note that the edge between the transfer of the 22nd and 23rd data words, is the last edge that the TXCLAV signal can change at the interface to the PHY chip (normally a SUNI chip in our designs). In our design we synchronize the TX-CLAV signal (using two back to back flops), this means we effectively need to be able to react to changes in TXCLAV up to the clock edge between data words 24 and 25 inside the APIC. The APIC is designed to tolerate changes up to the clock edge before it needs to assert the SOC signal.

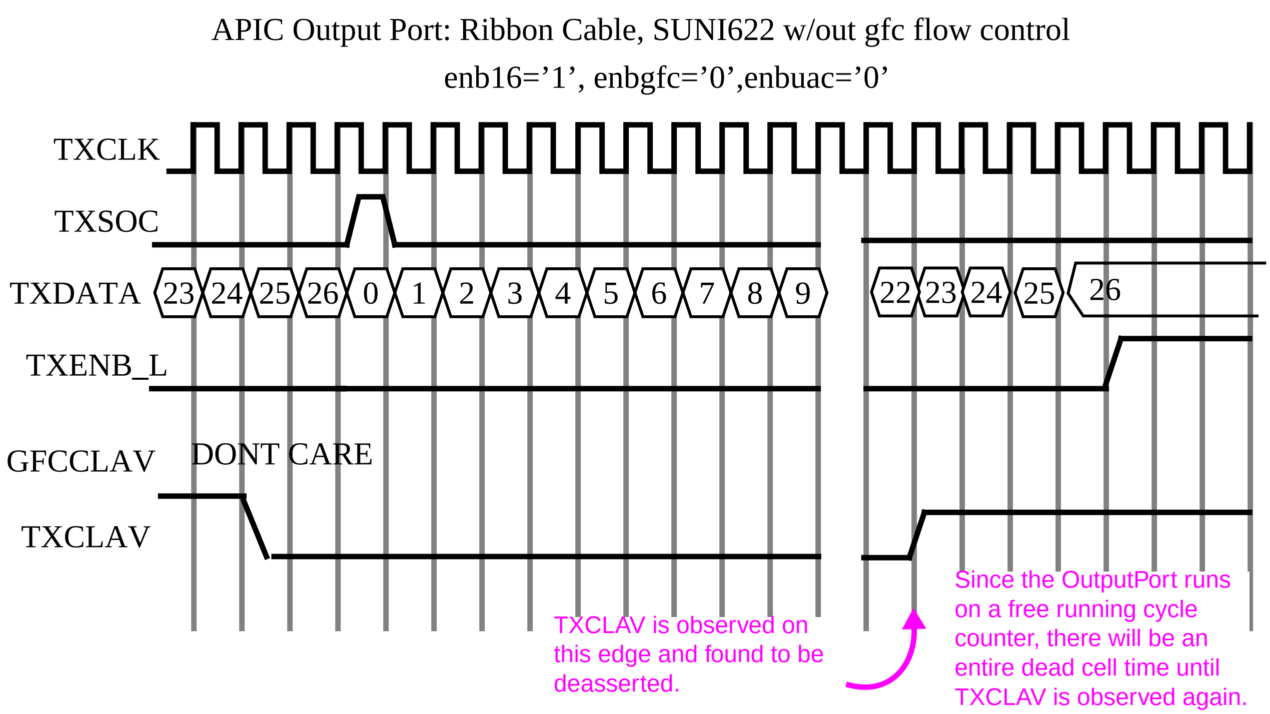

Figure 2: Timing Waveform of Output Port Interface

Below is the case where gfc flow control is enabled. In this case, both gfcclav and txclav are looked at to decide if a cell should be sent out. Otherwise the interface is the same.

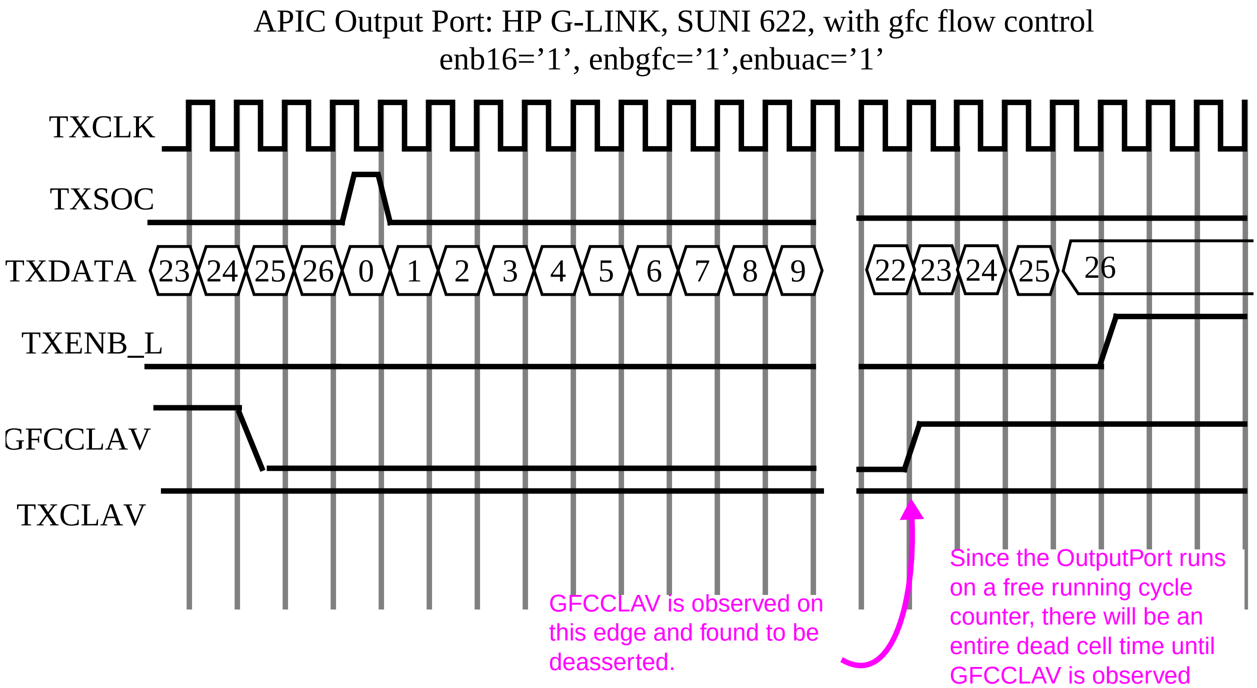

Figure 3: Timing Waveform of Output Port Interface

3 DataPath Implementation

The OutputPort uses some fairly simple logic in determining whether to send a cell, send a flow control cell (header all zeros except gfc which is given the value of generategfc from the VCXTRegblock and data all zeros), or send nothing. The following table will help in deciphering the options. The cell available column simply indicates if there is a cell waiting in the OutputSynch for transmission. ENBGFC indicates the level of the strap signal with the same name, when asserted GFC flow control is used. TXCLAV indicates the level of the pin flow control signal. Finally GFCCLAV indicates the level of the internal signal representing the current state of the GFC bit on incoming cells to the Input Port of the same link.

Cell Avail	ENB GFC	TX CLAV	GFC CLAV	Cell To Send
d	d	0	d	None (txclav is deasserted)
0	0	1	d	None (Not in GFC mode, and no cell to send)
1	0	1	d	Data (Data available and space available)
d	1	1	0	Flow Control Cell (GFC mode, space available, no gfcclav)
0	1	1	1	Flow Control Cell (GFC mode, space available, gfcclav, no cell to send)
1	1	1	1	Data (GFC mode, space available, gfcclav, cell available)

Note that in the last three cases in which 'enbgfc' is asserted, the gfc(0) bit of each cell will be filled in by the value of generategfc.

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The picture below shows a functional view of the OutputPort's data path. With a 16-bit UTOPIA interface, each word of the data from the OutputSynch comes in on the wordout bus every other cycle, for an 8-bit bus one 32-bit word is pulled from the OutputSynch every four cycles. When new data comes from the OutputSynch, it gets placed in the register wordtmp for 2 or 4 cycles. In the passing from input to 'wordtmp', the 28th bit of the first word of each cell (the gfc(0) bit), is possibly replaced by the generategfc signal if gfc flow control is enabled. In the next pipeline stage, the output of the wordtmp register is sent to the hecgen block for HEC generation while also passing into combinational logic. The combinational cloud in the OutputPort takes 32 bit word and either breaks it into 8-bit or 16-bit chunks. Additionally the combinational logic muxes in the HEC value on the 3rd (16-bit mode) or 5th (8-bit mode) word of the cell. Note this insertion of HEC results in a non-regular pulling of words from the OutputSynch (an extra wait cycle after the first 32-bit word is pulled). The HEC generator is document in the **HEC design document.**

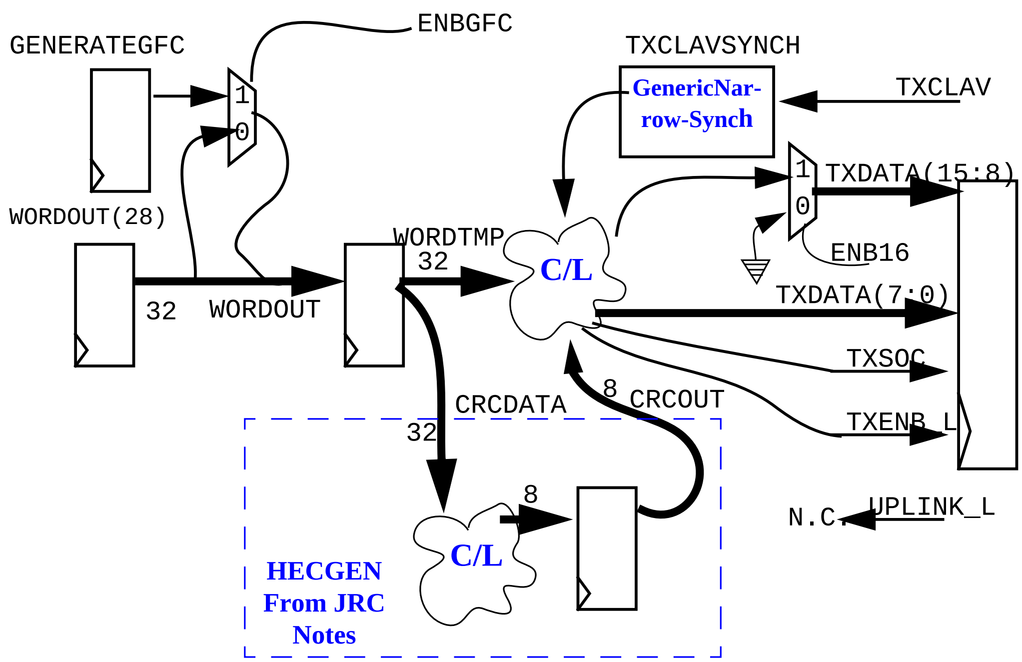

Figure 4: Internal Block Diagram of Output Port