

Homework 4

Assigned: 12/2/2004

Due Date: 12/9/2004

Directions

Be sure to explain any assumptions you make when solving the following problems. You will receive partial credit for incorrect answers only if your work is well-documented. You are encouraged to discuss concepts with your classmates, but the following problems must be completed individually. Start early so you have plenty of time to ask questions! Please submit questions that other students may have to the course bulletin board on the website.

1 Combinational Logic Design

Design and simulate a *divisible-by-three* detector. Your circuit will have four-bit input vector a and a single output bit x . Output x should be high if the binary number represented by the inputs is divisible by three. Write a logic equation for the output and use it to design a circuit using as few gates as you can (use only inverters, 2 input AND gates, OR gates, and XOR gates). Draw a logic diagram of the circuit.

2 Sequential Circuit Timing

Make your *divisible-by-three* detector a registered input/output circuit by placing edge-triggered D flip-flops at the inputs and output. (Each bit of the 4-bit input vector a will be connected to the D input of a flip-flop and the Q outputs will drive the combinational logic. The output of the combinational logic circuit will be connected to the D input of a flip-flop and the Q output will drive x .) Assuming the following timing characteristics for circuit components, determine the minimum clock period (maximum clock frequency) that can be used with this circuit. Does your circuit have a hold-time violation?

Times given in parenthesis denote variable gate delay, (*min*, *max*).

- $t_{CQ} = (0.8ns, 1.5ns)$
- $t_{setup} = 1.5ns$
- $t_{hold} = 1ns$
- $t_{NOT} = (0.4ns, 0.5ns)$
- $t_{AND} = (0.8ns, 1.1ns)$

- $t_{OR} = (0.7ns, 1ns)$
- $t_{XOR} = (1ns, 1.2ns)$