

## Addendum

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Washington University in St. Louis

## Memory Technology

- DRAM (Dynamic RAM)
  - » Main memory technology
  - » Very dense (1 bit = 1 transistor and 1 capacitor) and inexpensive
  - » Requires periodic refresh (by reading) → a Slows down overall speed
  - » Cycle time = 2 x Access time (Precharge Time)
- SRAM (Static RAM)
  - » Cache memory technology
  - » 4-6 transistors and 0 capacitors per bit →
    - No refresh period (no charge leakage)
    - No precharge time
    - Faster access time and Lower density

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## DRAM Burst Mode

- Operation: Load address; Read/Write data
- 5-5-5-5 Memory
  - » 5 cycles to read 8 bytes (two long integers); 20 cycles for 32 bytes
  - » 66 MHz Memory Bus → 75 ns = 5 x 15 ns to read 8 bytes
  - » If 100 MHz Memory Bus → 50 ns to read 8 bytes
  - » The 5 cycles includes cycle time and latency time
- 5-1-1-1 Memory (Burst Mode)
  - » Applies to consecutive memory accesses
  - » Best case: 8 cycles to get 32 bytes → 2 cycles for every 8 bytes
  - » Worst case: 5 cycles to get 8 bytes and rest

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## Thinker 2

```
int x[N];
for (int i=0; i<N/stride; i++){
  ++x[stride*i];
  stride += 1;      // or 2, 4, 8, ...
}
```

- Assume
  - » 100 MHz 5-1-1-1 SDRAM, 64-bit memory bus
  - » 1 GHz cache, 32-byte cache lines
  - » N so large that x[N] doesn't fit into cache
- Approximate total memory time when stride = 1?
- Average over N/stride accesses?
- Effect of stride?

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