





7. Consider the implementation of the previous function in a LookUp Table (LUT). Show each bit of the configuration memory for a LUT that implements:  
 $f(x, y, z) = x'yz + xy'z + xyz' + x'y'z'$ .

8. Show each bit of the configuration memory for a 4-input LUT that implements:  
 $f(w, x, y, z) = wx'yz + w'xy'z + wxz$

9. Using the diagram of the Virtex FPGA from the lecture notes, detail the implementation of a 9-input NAND gate in one slice of a CLB. Specify the function of each LUT.

10. Construct the decomposition chart for the function

$$f(w, x, y, z) = \sum(0, 1, 2, 3, 5, 6, 7)$$

Indicate all possible decompositions, and determine specifically the functions  $F$  and  $\Phi$  such that  $f(w, x, y, z)$  can be mapped into 2-input and 3-input LUTs.

11. The function  $f(v, w, x, y, z) = \sum(1, 2, 4, 7, 8, 11, 17, 19, 20, 22, 24, 26)$  can be decomposed to the form  $F[\Phi(v, y, z), w, x]$ . Determine the functions  $F$  and  $\Phi$ .