

CoE/EE460 Switching Theory

Lecture 1

Washington University
Spring 2001

<http://www.arl.wustl.edu/~lockwood/class/coe460/>

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Class Information

- **Location**
 - Lauderman 461
- **Class Time**
 - Monday / Wednesday
 - 2:37 – 4:00pm
- **Instructor**
 - Professor John W. Lockwood
 - Lockwood@arl.wustl.edu
 - Teaching Assistant: Henry Fu
 - hwf1@students.wustl.edu

Class Information (2)

- Website:
 - <http://www.arl.wustl.edu/~lockwood/class/coe460/>
- Newsgroup:
 - wu.ee.class.460
- Credits:
 - 3 units
 - Design: 1.2 units
 - Engineering science: 1.8 units

Class Information (3)

- Textbook
 - Gary D. Hachtel and Fabio Somenzi, *Logic Synthesis and Verification Algorithms*, Kluwer 1996
- Grading
 - Weekly Homeworks: 20%
 - Due every Wednesday before class
 - Exams: 40%
 - Two Exams
 - Final Exam: 40%

Course Outline (1)

- **Combinational techniques**
 - Boolean Algebras
 - Logic elements
 - Bilateral devices
 - Multiple output networks
 - Don't care conditions
 - Two-level Logic synthesis
 - Heuristic Minimization
 - Binary Decision Diagrams
- **Fault Analysis**
 - Fault detection,
 - System testing
 - Reliable design.

Course Outline (2)

- **Sequential techniques**
 - Finite state machines.
 - Synchronous circuits
 - Graph Algorithms
 - State assignment
 - State tables
 - Synthesis and verification
 - Finite Automata
 - Asynchronous circuits

Course Outline (3)

- Multi-level Logic Synthesis
 - Factored Forms
 - Multi-level minimization
 - Technology Mapping Sequential techniques
- Advanced Topics in Switching Theory

Design Automation

- Tools
 - Computer Aided Design (CAD)
 - Maps Hardware Description Language (HDL) into a technology
- Technology
 - Complementary Metal Oxide Semiconductor (CMOS)
 - Field Programmable Gate Arrays (FPGAs)

IC Design (1)

- Behavioral Synthesis
 - Extraction of logic from HDL

```
case(state) is
  when 0 =>
    if X = '1' then
      state <= 0; Z <= '0';
    else
      state <= 1; Z <= '0';
    end if;

  when 2 =>
    if X = '1' then
      state <= 0; Z <= '1';
    else
      state <= 1; Z <= '0';
    end if;

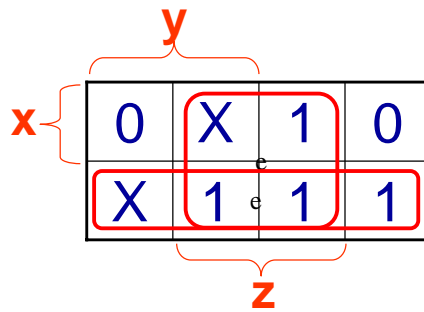
  when others => null;
end case;
```

IC Design (2)

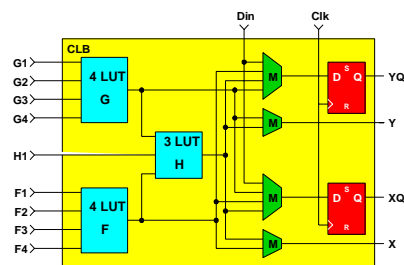
- Sequential Synthesis
 - Register movement
 - State Assignment & encoding

```
counter_process: process (CEN, counter) begin
  if CEN = '0' then
    nx_counter <= "0001";
  else
    nx_counter <= unsigned (counter) + 1;
  end if;
end process;
```

- Logic Synthesis
 - Logic minimization
 - Decomposition

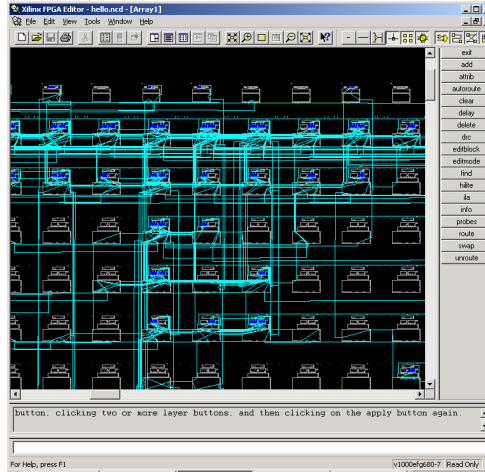


- Technology Mapping
 - Map function into library of gates
 - Timing optimization



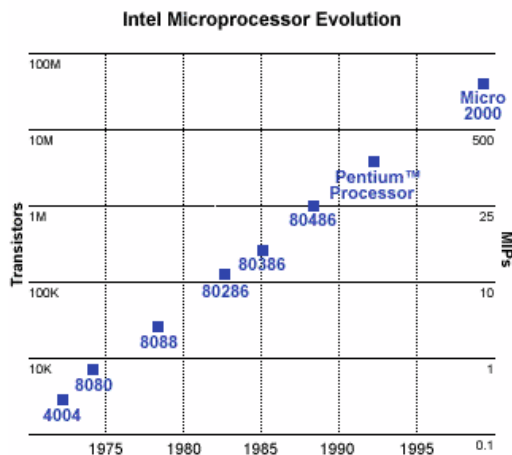
- Physical Design Synthesis

- Cell placement
- Routing



Moore's Law

- Microchip speed double every 18 months
- Number of Transistors/chips doubles every 18 months



Minimum Feature Size

- Length of CMOS gate
 - 1997: .25um (Pentium, K6)
 - Few Hundred MHz
 - 1999: .18um (Athlon, Pentium III)
 - GigaHertz
 - 2001: .13um (Pentium IV)
 - 2 GHz

Metrics of Optimal Logic Synthesis

- Critical Path Delay
 - Determines maximum frequency
 - Example:
 - Desktop Processor : 1100 MHz cost=\$400, 900MHz : Cost=\$90
 - Optimization
 - High frequency : Higher performance
- Area
 - Space used for logic + interconnect + I/O
 - Example:
 - $10\text{mm} \times 10\text{mm} = 100\text{mm}^2 = 1\text{cm}^2$
 - Optimization:
 - Smaller chip : Lower cost
- Power
 - Watts or mW
 - Example
 - Transmeta Courso – 2W
 - Optimization
 - Lower power : Longer battery life

Area/Time Tradeoffs

- **Factors**

- Area = logic size + routing area
 - Additional gates improves performance
- Delay = computation time + routing Delay
 - Longer Delay = Slower Frequency

- **Constraints**

- Area of logic and routing must fit within chip
- Circuit must meet timing

- **Balanced Design**

