

CoE/EE460 Switching Theory

Lecture 13

Washington University
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<http://www.arl.wustl.edu/~lockwood/class/coe460/>

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Announcements

- Homework 4
 - Points lost for missing e-f-g-h-i-j
 - Resubmit to Henry before Wednesday for credit
- Homework 5
 - Problems 1 - 4 require 3 Solutions
 - NMOS + resistor(s) only
 - PMOS + resistor(s) only
 - NMOS + PMOS = CMOS only
 - Problem
 - Consider 2LUT, 3LUT Solution
 - Consider 3LUT, 2LUT Solution

Binary Decision Diagrams (BDDs)

- Properties of BDDs
 - Canonical
 - Same circuits will have same BDD
 - Assuming the same ordering of terms!
 - Effective for large sets
- Chapter 6 of text

Directed Acyclic Graph (DAG)

- Directed Acyclic Graph (DAG)
 - Directed
 - Edges are of one direction
 - Acyclic
 - No cycles between Nodes
- Binary Decision Diagram
 - Nodes are Multiplexors
 - Root node is the function
 - Leaf nodes are {0,1}
 - Literals are the selectors

BDD Example

- Example:
 - Multiplexor circuit of $f(a,b,c)$
 - Edges labeled
 - $\{1,0\}$ or
 - $\{\text{Then,Else}\}$ or
 - $\{\text{---,-o-}\}$
 - *Support* of Node
 - Variables that node depends on
- Example:
 - Show BDDs for Typical Functions (p224)

Creating a BDD (1)

- Choose an Order
 - Ordered BDD
 - Literals appear in same order along all paths from root to leaves
 - Prefer largest split first
- Generate Root Node
 - Apply Boole's Expansion Theorem to find Root
 - $\text{Root} = f(a,b,c) = f_a(a=1,b,c) + f_a(a=0,b,c)$
 - Combine if $f_a = f_a'$
 - Example
 - $f(a,b,c) = abc + b'd + c'd$

Creating a BDD (2)

- Apply Boole's Expansion Again
 - Generate Next-Level Node
 - $(f_a)_b = f_{ab}$
 - $(f_a)_{b'} = f_{ab'}$
 - $(f_{a'})_b = f_{a'b}$
 - $(f_{a'})_{b'} = f_{a'b'}$
 - Combine identical f_{xy} results
 - Example (p.225)
 - $f(a,b,c) = abc + b'd + c'd$
 - $f(b,c) = a*f_a(b,c) + a'*f_{a'}(b,c)$
 - $(f_{a'})_{b'}$

Reduced BDDs

- Isomorphic Graphs
- Identify isomorphic subgraphs
 - Remove redundant nodes
- Ordering
 - $F(a,b,c,d,e,f) = ab + cd + ef$
 - Try $F(a,c,e,b,d,f)$