

CS/CoE 535

Acceleration of Networking Algorithms in Reconfigurable Hardware

Lecture 17

Washington University
Fall 2001

<http://www.arl.wustl.edu/~lockwood/class/cs535/>

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Announcements : Upcoming Deadlines

- Wednesday 11/28/01 (Today)
 - In-Class Status presentations
- Wednesday 12/5/01 (1 Week)
 - In-Class Project Presentations (See Lecture 16)
 - Submit Peer Evaluation Forms
- Friday 12/7/01
 - Andre DeHon, Caltech : Colloquium Talk
 - “Score: A Compute Model for Reconfigurable Systems”
 - 11am on Friday, December 7 in Lopata 101
- Monday 12/10/01
 - Homework 3 Due
 - Covers Colloquium talk (above) and in-class presentations
- Wednesday 12/12/01 :
 - Final Project Written Reports Due (See Lecture 15)
- Friday 12/21/01
 - DAC Design Contest Deadline

Upcoming Colloquium Talk : Friday 12/07/01

“Score: A Compute Model for Reconfigurable Systems”

Andre DeHon, Caltech

11am on Friday, December 7 in Lopata 101

- A primary impediment to wide-spread exploitation of reconfigurable computing is the lack of a unifying computational model which allows application portability and longevity without sacrificing a substantial fraction of the raw capabilities. To address this problem, we are developing SCORE (Stream Computation Organized for Reconfigurable Execution), a stream-based compute model which virtualizes reconfigurable computing resources (compute, storage, and communication) by dividing a computation up into fixed-size “pages” and time-multiplexing the virtual pages on available physical hardware. Consequently, SCORE applications can scale up or down automatically to exploit a wide range of hardware sizes. We hypothesize that the SCORE model will ease development and deployment of reconfigurable applications and expand the range of applications which can benefit from reconfigurable execution. Further, we believe that a well engineered SCORE implementation can be efficient, wasting little of the capabilities of the raw hardware.
The SCORE model exposes more of the freedom which exists in applications, creating additional opportunities for mapping and optimization. While we have developed SCORE initially with reconfigurable systems in mind, the model is not limited to reconfigurables and may provide a reasonable model for capturing computations for a large range of modern, scalable, chip architectures.

BIO:

Andre' DeHon is an Assistant Professor of Computer Science at the California Institute of Technology. He holds S.B. and S.M. and Ph.D. degrees from MIT. During his MIT work, he lead the development of the DPGA, TSFPGA, and MATRIX architectures. From 1996-1999, Dr. DeHon co-ran the Berkeley Reconfigurable Architecture, Software, and Systems (BRASS) group at UCB along with Prof. John Wawrzynek, working on efficient, high-speed spatial architectures (HSRA), hybrid architectures which combine temporal (RISC processor) and spatial processing, computational models for these devices (SCORE), and mapping software for these devices.

39th DAC Student Design Contest

• The 39th DAC Student Design Contest

– Submissions Open : Now : Deadline, December 21, 2001

- The contest will allow entries of both integrated circuits and electronic systems (board-level design). It will have two categories: 'Conceptual' and 'Operational.'
 - Operational designs will have been implemented and tested. Proof of implementation in the form of die- or board-photographs and measurement data must be supplied.
 - Conceptual designs need not have been implemented but must have been thoroughly simulated and must include a test plan.
- CRITERIA FOR ENTERING THE CONTEST
 - Submissions are invited from full-time graduate and undergraduate students. The design must have taken place as part of the students' course or research work at the university and must have been completed within 18 months prior to the submission deadline.
 - Submissions are made electronically via the DAC web site. Submissions include two files. The first is the title and a 60-word abstract. The second is a document describing the design not exceeding 6000 words, with a recommended length of 4000 words. The deadline for submission is December 21, 2001.
 - Submissions are judged by a panel of experts including members of the DAC Technical Program Committee and other representatives from industry. Judging criteria include originality, soundness of engineering, measured performance and the quality of the written submission. Winners will be notified in mid-February.
- Details: <http://www.dac.com/39th/studcon.html>

Project Notes for Peer Evaluation Form

Peer Evaluation

- Use a 10-point scale to evaluate each project on the categories specified.
- Evaluate all projects that you observed (including your own)
- Justify your ratings with comments

10-point scale	Categories
10: Excellent 9-6: Good 5: Average 4-1: Poor 0: Terrible	<ul style="list-style-type: none"> Technical Merit: Rate the projects difficulty. To what degree has the team demonstrated thought, planning, and programming to solve a challenging problem? Accomplishments: Rate the implementation. Does the program work as specified. Does the project as a whole represent a significant programming effort? Is the amount of work proportional to the size of the team? How much of the work is original? Comments: Provide specific reasons why you scored the project as you did. Constructive and specific remarks are most helpful.

Project Title	Technical Merit	Accomplishments	Comments
DRR Scheduling for SAR'd packets	10	7	
Fair Queuing Module	?	?	
IDE Interface as FFX Module	?	?	
IPv6 Tunneling Over an IPv4 Network	?	?	
Motion JPEG Decoder for MMX Image Proc.	?	?	
Network Traffic Generator	?	?	
Optic Flow Acceleration Using FPGA HW	?	?	
Power use for numeric representation	?	?	
Segmentation and Reassembly of Packets	?	?	
Tree-based IP packet filter	?	?	
Video Scaling in Reprogrammable Hardware	?	?	

- Take notes during today's presentation
- Electronically submit form after all projects have been presented.