

CS/CoE 535

Acceleration of Networking Algorithms in Reconfigurable Hardware

Lecture 3

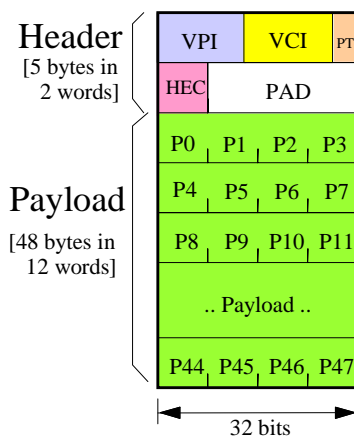
Washington University
Fall 2001

<http://www.arl.wustl.edu/~lockwood/class/cs535/>

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Includes timing diagrams by David Taylor

ATM Cell Format



• Header

- VPI: Virtual Path Identifier
 - 12 bits [31 downto 20] of Word 0
- VCI: Virtual Circuit Identifier
 - 16 bits [19 downto 4] of Word 0
- PT: Payload Type
 - 4 bits [3 downto 0] of Word 0
- HEC: Header Error Check
 - 8 bits [31 downto 24] of Word 1
- PAD: Padding
 - 24 bits [23 downto 0] of Word 1

• Payload

- P0 .. P47

MP1 Problem Statement

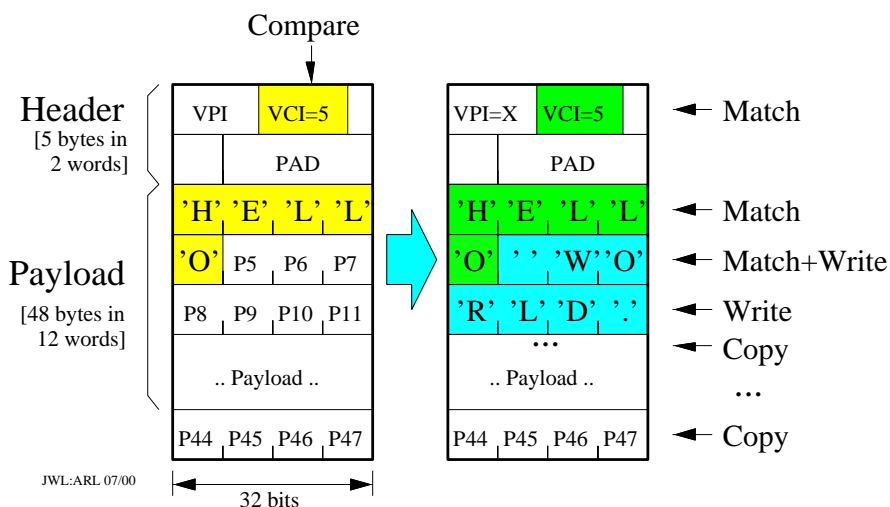
- **General Statement**

- “Implement a plug-in module that monitors a traffic flow. For cells with payloads that begin with “Hello”, have the module replace the following bytes with “World”.

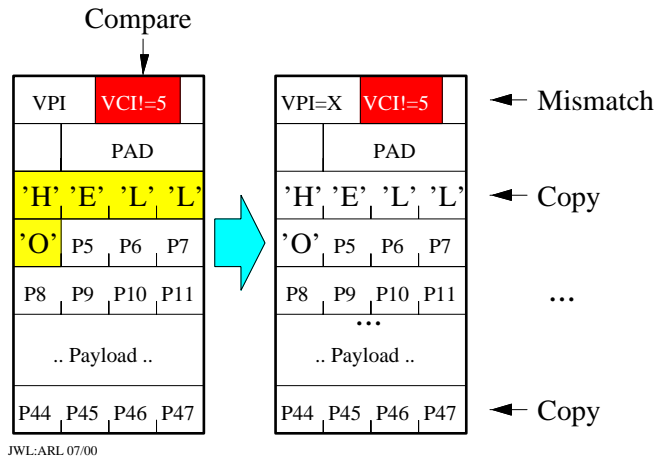
- **Details**

- Scan Flows on VCI=5
- Match the content of the cell for the “HELLO”
 - **ASCII: “HELLO”**
 - **Hex: 48 – 45 – 4C – 4C – 4F**
 - **Binary: 0100,1000 - 0100,0101- 0100,1100 - 0100,1100 - 0100,1111**
- Replace following contents with “WORLD.”
 - **ASCII “WORLD.”**
 - **Hex: 57 – 4F – 52 – 4C – 44 – 2E**
 - **Binary: 0101,0111 – 0100,1111 – 0101,0010 – 0100,1100 – 0100,0100 – 0010,1110**

“Hello, World” Module Function

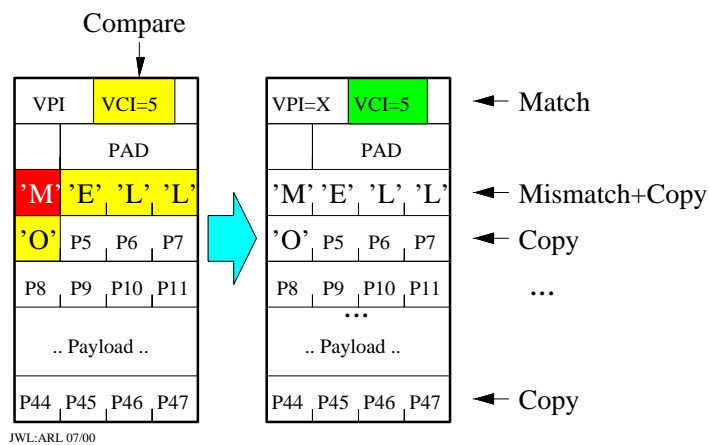


Case 1: Mismatched VCI



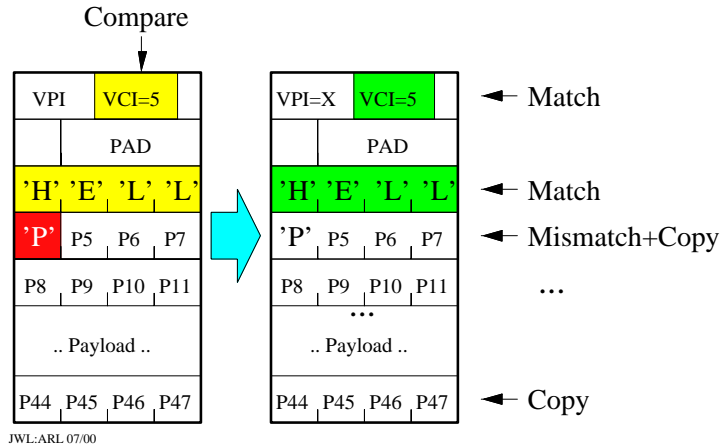
- Only process Cells on the selected VCI
 - All other flows should pass unchanged

Case 2: Mismatched Source String



- Cell payload must contain “HELLO” in payload.
 - “MELLO” ≠ “HELLO”

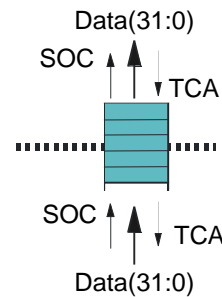
Case 3: Mismatched Source String [word 2]



- Payload must match over entire string.
 - Data arrives as streaming words

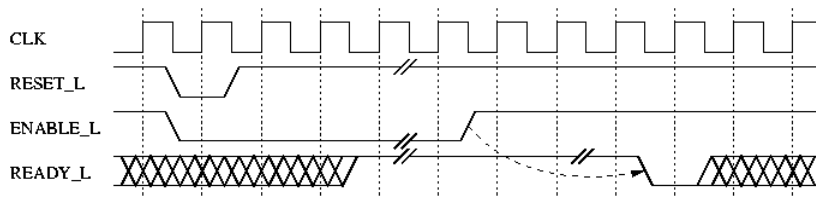
Cell Interface

- Signals
 - Data(31:0)
 - Cell data
 - Start of Cell (SOC)
 - Indicates first word
 - Transmit Cell Available (TCA)
 - Congestion Feedback



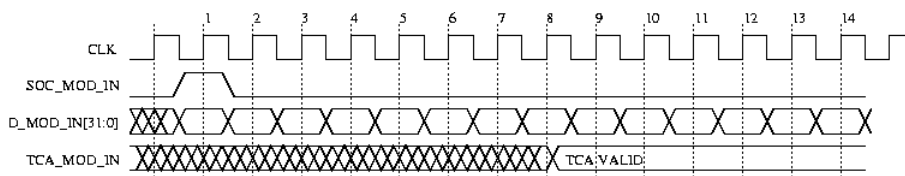
Control Interface

- 100MHz global clock (CLK)
 - All I/O signals should be synchronous to CLK
- Synchronous reset (RESET_L)
 - Asserted low for 1 clock cycle



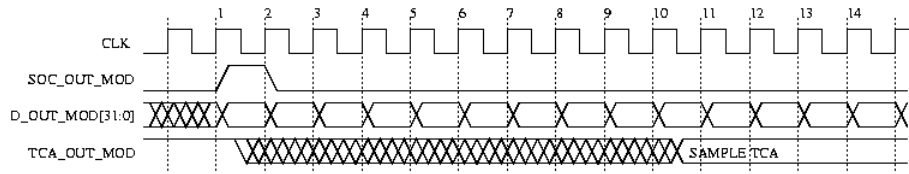
Cell Input Interface

- Start of Cell (SOC_MOD_IN)
 - Signals the first word of the ATM cell
- 32-bit wide data path (D_MOD_IN)
 - ATM cells transferred as (14) 32-bit words
 - First word arrives with SOC_MOD_IN
 - Remaining 13 words arrive on subsequent clock cycles
- Transmit Cell Available (TCA_MOD_IN)
 - Signals module's ability to accept a cell
 - Must be valid 6 clock cycles prior to the last cycle of the current cell transfer



Cell Output Interface

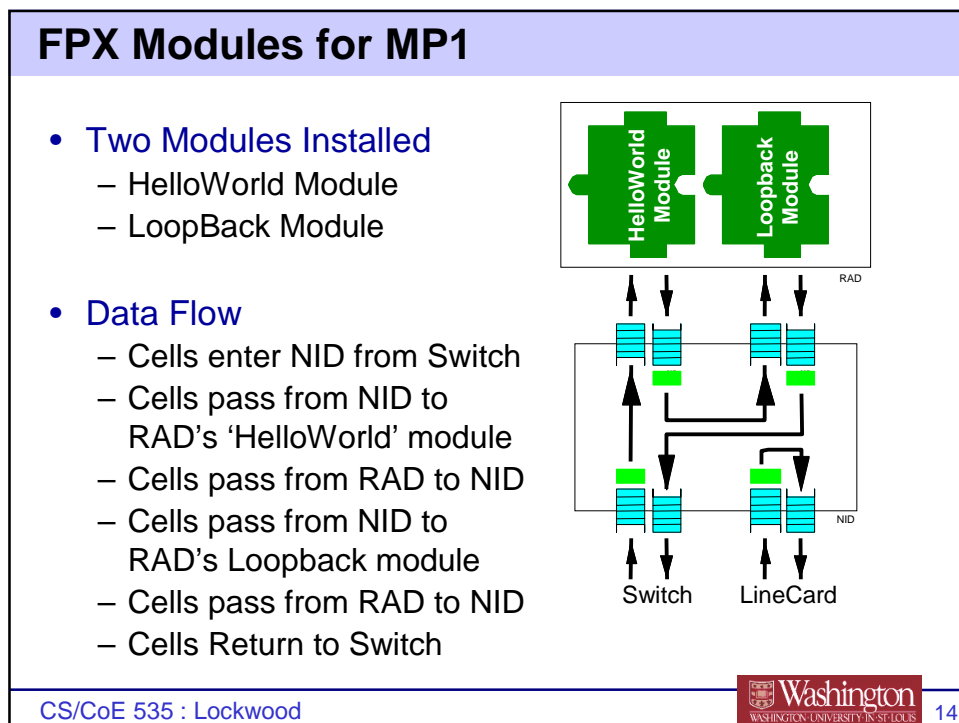
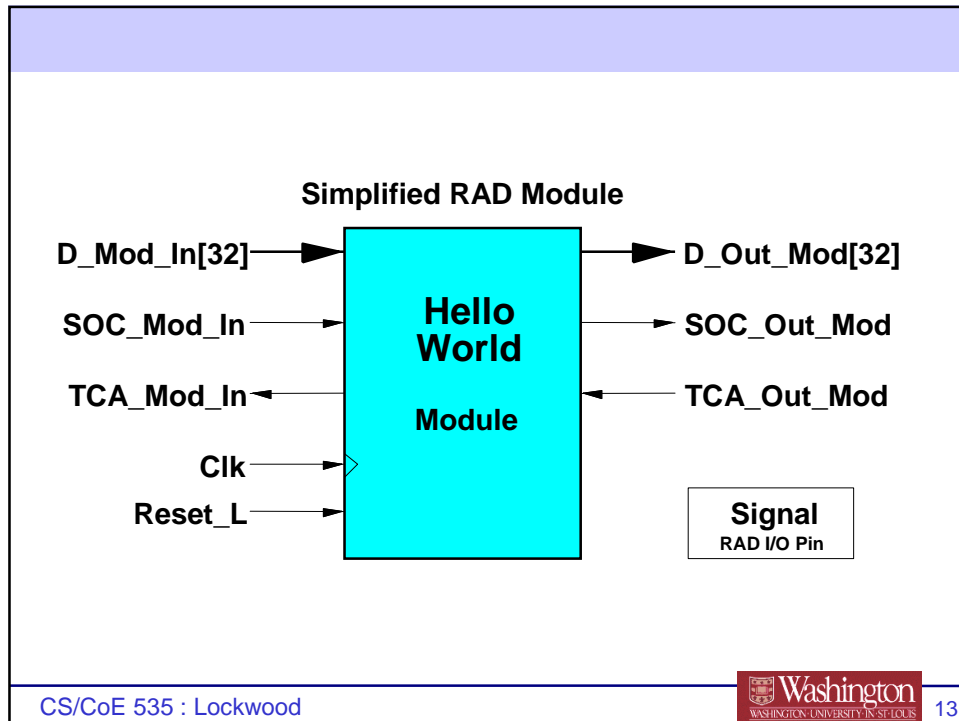
- **Start of Cell (SOC_OUT_MOD)**
 - Signals the first word of the ATM cell
- **32-bit wide data path (D_OUT_MOD)**
 - ATM cells transferred as (14) 32-bit words
 - First word sent with SOC_MOD_IN
 - Remaining 13 words sent on subsequent clock cycles
- **Transmit Cell Available (TCA_OUT_MOD)**
 - Signals output's ability to accept a cell
 - Modules must sample TCA_OUT_MOD no sooner than 3 clock cycles prior to asserting SOC_OUT_MOD



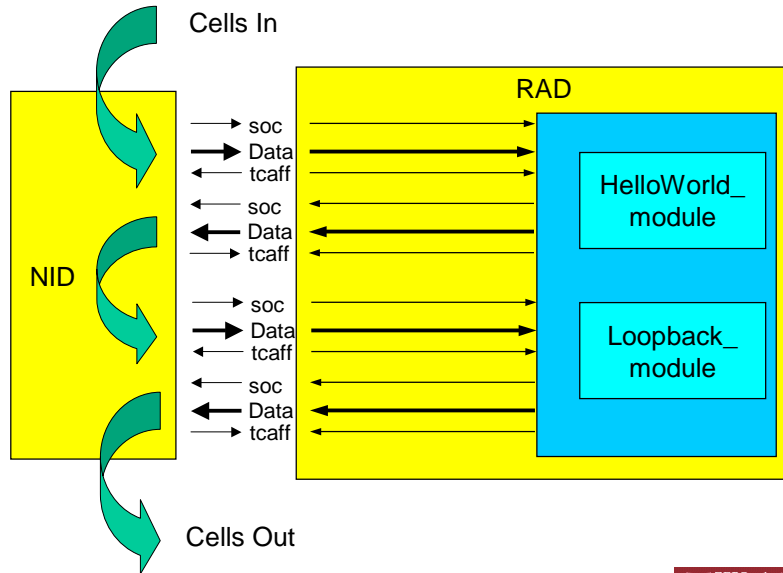
Reference: Hex / ASCII Table

"Hex.txt" 34 lines, 1776 characters

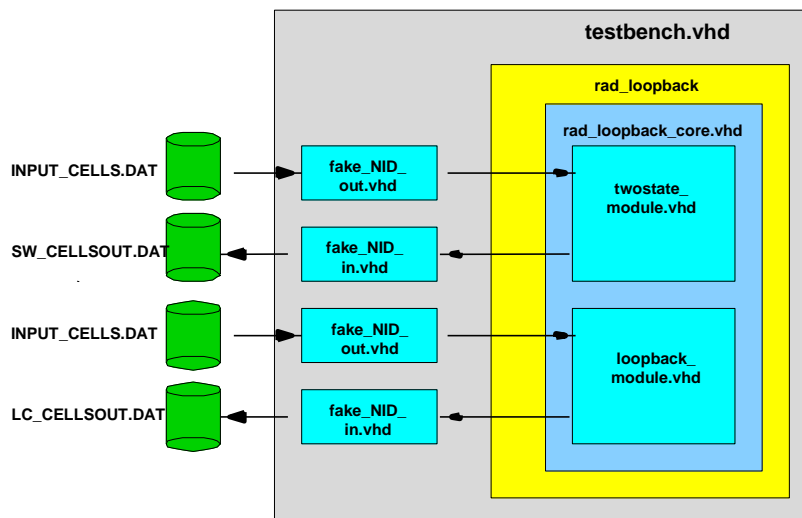
Hx Symbol (Function)	Hx Char	Hx Char	Hx Char
00 NUL (null)	20 SPACE	40 @	60 `
01 SOH (start of head)	21 !	41 A	61 a
02 STX (start of text)	22 "	42 B	62 b
03 ETX (end of text)	23 #	43 C	63 c
04 EOT (end of trans)	24 \$	44 D	64 d
05 ENQ (enquiry)	25 %	45 E	65 e
06 ACK (acknowledge)	26 &	46 F	66 f
07 BEL (bell)	27 '	47 G	67 g
08 BS (backspace)	28 (48 H	68 h
09 TAB (horizontal tab)	29)	49 I	69 i
0A LF (line feed)	2A *	4A J	6A j
0B VT (vertical tab)	2B +	4B K	6B k
0C FF (form feed)	2C ,	4C L	6C l
0D CR (carriage ret)	2D -	4D M	6D m
0E SO (shift out)	2E .	4E N	6E n
0F SI (shift in)	2F /	4F O	6F o
10 DLE (escape)	30 0	50 P	70 p
11 DC1 (devcontrol 1)	31 1	51 Q	71 q
12 DC2 (devcontrol 2)	32 2	52 R	72 r
13 DC3 (devcontrol 3)	33 3	53 S	73 s
14 DC4 (devcontrol 4)	34 4	54 T	74 t
15 NAK (nak)	35 5	55 U	75 u
16 SYN (synch idle)	36 6	56 V	76 v
17 ETB (end of block)	37 7	57 W	77 w
18 CAN (cancel)	38 8	58 X	78 x
19 EM (end of medium)	39 9	59 Y	79 y
1A SUB (substitute)	3A :	5A Z	7A z
1B ESC (escape)	3B ;	5B [7B {
1C FS (file separator)	3C <	5C \	7C
1D GS (group sep)	3D =	5D]	7D }
1E RS (record sep)	3E >	5E ^	7E ~
1F US (unit sep)	3F ?	5F _	7F DEL



Data Flow for MP1



ModelSim Testbench for MP1



Contents of TESTCELL.DAT

```
new_cell           Indicates new cell
00000050          VCI=5
E2000000
48454C4C          1st Payload word = "HELL"
4F000000          2nd Payload word = "O"
00000000
00000031
00000032
00000033
00000034
00000035
00000036
00000037
00000038
00000039
```

Contents of TESTCELL.DAT(continued)

```
new_cell           Indicates new cell
00000040          VCI = 4
92000000
48454C4C          1st Payload word = "HELL"
4F000000          2nd Payload word = "O"
00000000
00000031
00000032
00000033
00000034
00000035
00000036
00000037
00000038
00000039
```