

CS6811: Research Seminar on Reconfigurable Hardware

Lockwood : Spring 2002

Review of: Jbits: Java based interface for reconfigurable computing

- Paper by:

- Steve Guccione, Delon Levi and Prasanna Sundararajan (XILINX Inc.)

- 2nd Annual Military and Aerospace Applications of Programmable Devices and Technologies Conference (MAPLD), 1999

- (next one, in Laurel, Maryland, on Sept 10-12, papers due May 28th: http://klabs.org/richcontent/MAPLDCon02/MAPLDCon02_CFP.html)

- On-line as:

- <http://www.io.com/~guccione/Papers/MAPPLD/JBitsMAPPLD.pdf>

- Summarized by: Edson L. Horta

Style of Writing

- “Marketing Paper”

- 3 self-references (FPL97,2xSPIE98)
 - 2 Xilinx literature

- Revisor Notes

- Where is the second piece on the last paragraph of page 3?

- Two sections 4

- The first one could be placed at the end of the paper (as it was in the XBI paper!!). The author used it to call the Boardscope section.

Introduction

- JBits – Java classes API used to access Xilinx FPGAs resources
- Evolution
 - JERC6K (Java Environment for Reconfigurable Computing in XC6200)
 - XBI (Xilinx Bitstream Interface) for XC4000
 - JBITS (XC4000 and VIRTEX)
- Design Flow (Figure 1)
 - A library of configurable architectural features of the FPGA
 - The user provides Java code to join the features and generate a configuration bitstream

JBits System Design (Fig 2)

- User Java Application interfaces with
 - Core Library – Java classes used to define macrocells or cores (adders, counters, multipliers, etc)
 - JBits
 - XHWIF – Java interface to communicate with FPGA-based boards
- JBits Limitations
 - Source code includes everything, even the routing (possible solution: pre-constructed macrocells)
 - User must know the FPGA architecture
 - Timing analysis is not possible (JBits is in the end of the tool chain)

Boardscope (Fig 4)

- FPGAs' ICE (In-Circuit Emulator)
 - Uses JBits interface to FPGA bitstream
 - Uses XHWIF to interface with the FPGA board
 - View the state of CLBs
 - User Interface (Fig 5)
 - Reset
 - Step
 - Load Display
 - File

XHWIF

- Xilinx Hardware Interface Standard
 - Java interface to communicate with FPGA-based boards
 - Read/write bitstreams
 - Types and numbers of FPGAs on the board
 - Access to on-board memories
 - Access to on-board clock
- XHWIF Server
 - Implements a XHWIF via TCP/IP
 - Enables remote design development

Conclusions

- JBits Environment (Fig 7)
- RTR using JBits
 - calls to JBits to modify the bitstream
 - Calls to XHWIF to interact with the hardware

Future Work (not so Future!!!)

- Routing API (JRoute – RAW2000)
(<http://ipdps.eece.unm.edu/2000/raw/18000876.pdf>)
- Hardware Simulator (VirtexDS – SPIE2000)
(<http://www.io.com/~guccione/Papers/VirtexDS/simulator.ps.gz>)
- Extensive parameterizable cores API
(<http://www.io.com/~guccione/Papers/RtpCores/RtpCores.pdf>)
- JRTR (not mentioned in the paper)
(<http://www.io.com/~guccione/Papers/JRTR/partial.pdf>)
 - Caches the configuration data
 - Modifies only the necessary bits to partial reconfigure the FPGA

JBits x PARBIT

- PARBIT
 - Manipulates bitstreams generated by bitgen

PARBIT	JBits
XCV50E, XCV100E, XCV200E, XCV300E, XCV400E, XCV405E, XCV600E, XCV812E, XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E	XCV100, XCV1000, XCV150, XCV200, XCV300, XCV400, XCV50, XCV600, XCV800
No software running	Needs Java SDK 1.2.2 running
Any Programming Interface	XHWIF