CSE460
Switching Theory

Lecture 17 : Final Exam and Future Directions

Washington University
Spring 2001

http://www.arl.wustl.edu/~lockwood/class/cse460/

Final Exam

- Thursday – May 4 (in class)
  - Covers:
    - All Lectures
    - Material referenced in textbook
    - Homeworks
  - You may bring (only):
    - Boolean Algebra Theorems & Postulates sheet (on web)
    - Your own 2 pages of [2 sided] note sheets
  - You may not bring
    - Textbook
      - This is closed-book exam
    - Computation or communication device
      - Problems will be sufficiently small to work by hand

Lecture Material (1-4)

- Lecture 1 : January 17, 2006
  - Course Information,
  - Motivation for Logic Synthesis and CAD
  - Metrics of circuit implementation
  - Reading Assignment: Hachtel: Chapter 1, Sections 1.1 - 1.4
- Lecture 2
  - Sets
  - Cardinality
  - Karnaugh Maps of 2-5 Variables
  - Basic Set Operators & Relations
  - Reading Assignment: Hachtel: Chapter 3 (All)
- Lecture 3
  - Partial Orders
  - Hasse Diagrams
  - Meet / Join / Poset
  - Ordered Sets
  - Lattice
- Lecture 4
  - Boolean Functions
  - Boole's Expansion Theorem
  - Minterms & Maxterms
  - Atoms
  - Reading Assignment: Hachtel: Chapter 4 (All)

Lecture Material (5-8)

- Lecture 5
  - Satisfiability Don't Care
  - Incomplete specification
- Lecture 6
  - Implicants
  - Prime Implicants
  - Essential Prime Implicants
  - Unate Covering Problem
  - Quine's Theorem
- Lecture 7
  - Computational Techniques for logic minimization (1)
  - Representation of logic functions on computers
  - Bit-wise operators on logical values
- Lecture 8
  - Computational Techniques for logic minization (2)
  - Organization of SOP groups
  - Operations on SOP groups
  - Organization of groups in table
  - Display of a functions resulting prime implicants

Lecture Material (9-11)

- Lecture 9
  - Finding Essential Prime Implicants
  - Optimizing with Don't Care Inputs
  - Greedy Selection
  - Branch and Bound
- Lecture 10
  - Design Flow: Technology independent and dependent phases
  - FPGA and LookUp Table (LUT) technologies
  - Lookup Table function mapping
  - Decomposition
- Lecture 11
  - Chortle Algorithm for K-input LUT mapping
    - Dynamic Programming Algorithm
    - Developed by R. Francis, J. Rose, K. Chung, Z. Vranesic (1990s)
    - Calculation of MinMap: Minimum Cost to implement sub-circuit
    - Utilization Division for a subtree

Lecture Material (12-14

- Lecture 12
  - Binary Decision Diagrams (BDDs)
    - Creation using Boole's Expansion Theorem
    - Support Functions
    - Variations with term Ordering
    - Relationship to Decomposition
- Lecture 13
  - Synchronous Circuits
  - Finite State Machines (FSMs)
  - CLB Mapping of combinatorial logic and state.
  - Informal Synthesis Techniques
- Lecture 14
  - FSM Equivalence
  - Partition/Refinement Algorithm
  - State minimization

Lecture Material 15-16

- Lecture 15
  - State Identification
  - Homing Sequences
  - Synchronizing Sequences
  - Distinguishing Sequences
- Lecture 16
  - Deterministic Finite Automata (DFA)
  - Non-deterministic Finite Automata (NFA)

Types of Questions

- Boolean Equation Proofs
- Relation Matrix Properties
- Logic Intervals
- LUT Mapping
- Decomposition
- Prime Implicants and Essential Prime Implicants
- Chortle
- Finite State Machines
- FSM Partition Methods

Where to do from here?

- Where to go from here?
  - Classes next fall
    - CSE 566: Gaming System on Programmable Chip
  - Graduate School
    - Computer Engineering
    - Computer Science
  - Industry
    - ASIC Design, Design Automation, Hardware Engineering
    - Xilinx, Altera, Intel, Cisco, Nortel, TI, Motorola, Others