

Advanced Computer Systems Architecture

Chip-Multiprocessors: Applications and Architectures

CSE 526M

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Plan for Today

- Announcements
 - Office hour change: Tu, 3-4pm
 - Today: 3-3:45pm
- Questions
- Today's discussion

Project Logistics

- Dates
 - Today's date: Apr 6
 - End date: **(1.5 weeks later)** Thursday, April 15
- Weekly Milestones

M1	Mar 4	Implementation 1
M2	Mar 18	Implementation 2
M3	Mar 25	Implementation 3
M4	Apr 1	Implementation Wrap-up
M5	Apr 8	Plan future work, Reports
M6	Apr 15	Presentations

The Case for RISC

- Observation: computers are getting more complex
- The Case
 - Reasons for Complexity
 - CISC Usage
 - Consequences of CISC
 - RISC and VLSI
 - High-Level Language Computer System
 - RISC History
- The Intel IXP

Computers are Getting More Complex

- Newer machines of the time (from IBM and DEC) had a larger set of architectural features than their predecessors
- Authors contend that they are less cost-effective as a result of their increased complexity

Reasons for Complexity

- Memory vs. CPU Speeds
 - CPUs were 10x faster than memory
- Microcode and LSI Technology
 - With microcoding, it's cheap to “move subroutines into the architecture”
- Code Density
 - Expensive memory inspires small programs
- Marketing Strategy
 - Number and “power” of instructions were a selling point

Reasons for Complexity (2)

- Upward Compatibility
 - Instruction sets only grow
- Support for High Level Languages
 - High-level languages reduce the cost of software, and computer companies want to help
- Use of Multiprogramming
 - Handling interrupts and context switches require additional support

CISC Usage

- Programmed by compilers, not humans
- Compilers only use a fraction of CISC instruction set!
- Implication: why bother with the unused, or infrequently used, instructions?

Consequences of CISC

- Faster memory
 - “Semiconductor memories are both fast and relatively inexpensive.”
- Irrational implementations
 - Complex instructions can be slower than their simpler counterparts
 - E.g., in IBM 370, 3 loads is faster than 1 load_3

Consequences of CISC (2)

- Lengthened design time
 - Programs may not use all instructions, but you have to design, implement, validate and test them all
- Increased design errors
 - More complexity means more opportunity for error

RISC and VLSI

- Perspective: single-chip VLSI computers were the wave of the future
- Implementation feasibility
 - A simpler chip is more likely to fit on-chip
- Design time
 - Chip density in VLSI doubles every 2 years, thus that should be the target design and debug cycle
 - Simpler RISC chips are better suited to this (mostly due to reduced debugging time)

RISC and VLSI (2)

- Speed
 - RISC involves simpler circuits, simpler control logic; this implies a faster clock
- Better use of chip area
 - Use reclaimed chip area for
 - On-chip caches
 - Larger and faster transistors
 - Or even *pipelining*
 - RISC will stay one step ahead of CISC

High-Level Language Computer System

- Goal of HLLCS: user only interacts via HLLs
- Authors contend: use RISC processor, provide HLL through compilers and software systems (rather than an HLL interface at the processor)

RISC History

- At the time of publication
 - Berkeley “told the story”
 - IBM & Bell Labs “did the work”
- Eventually
 - Berkeley and Stanford both built chips
 - MIPS and SUN were side-effects

Considering the IXP

- Is the IXP ME RISC or CISC? Explain your answer.
- This paper predates single-chip VLSI computers (e.g., microprocessors).
 - What new concerns have emerged in the microprocessor age?
 - How do these impact microprocessor design?
- Microprocessors are no longer the wave of the future. What is?

IXP: RISC or CISC?

- Small number of instructions
- Some are special purpose
 - Reasons for complexity?
 - How are they used?
- Small, simple implementation
- Pipelined implementation
- HLL support?
- Verdict: RISC

Concerns in the Microprocessor Age

- Software costs dominate
 - Stable ISAs
 - Mature compilers, tools
 - Binary compatibility
 - If you have to recompile, why not choose another architecture?
- Platform based on commodity pieces
 - I/O buses
 - I/O devices
 - Motherboards
 - Except: CPU, graphics card
- Memory is slow, inexpensive
- Disk is even slower and less expensive

Waves of the future

- Systems on a chip (SOC)
 - CPU, I/O and memory controllers, memory, special-purpose circuits, radios
 - With billions of transistors, the whole system fits on a chip
 - Pin counts and power are dominant concerns
 - The **single-chip VLSI system** is a bigger leap than the **single-chip VLSI computer** was
- Chip-multiprocessors
 - Soon, all microprocessors will be chip-multiprocessors
 - What does this mean for binary compatibility and stable ISAs?

Assignment

- Thursday (4/8)
 - **Commentary:** *Instruction Sets and Beyond: Computers, Complexity and Controversy*
 - **Milestone 5:** Reports
- Tuesday (4/6):
 - First 3 presentations
 - ACL-based Firewall
 - DDOS Shield
 - Bloom Filter