Design of a Flexible Open Platform for High Performance Active Networks

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http://www.arl.wustl.edu/arl/
Motivation

- Technology advances adding new functionality to internet routers.
  - logic capabilities growing much faster than IO
  - packet classification, per flow queueing becoming common
  - single chip packet processing engines with 16 processors now becoming available

- Application-specific processing in routers could become routine.
  - active networking is one way to exploit trend
  - alternative model
    - signalling and resource reservation
    - packet classification and flow-specific routing

- Key challenge is application software.
- Need better experimental platforms for researchers.
Towards an Open Internet Router

- Modular components.
  - ability to swap components - both hardware and software
    - routing, signalling, management software
    - address lookup and packet classification
    - queueing and packet scheduling
  - open, documented and straightforward interfaces

- Dynamic insertion of application-specific processing.
  - active networking model and others

- High performance.
  - gigabit links and scalability to large numbers of ports
  - packet processing rates of at least a million/second per link
  - application-specific processing on large fraction of traffic
  - need **credible demonstrations** to influence commercial practice
Active Router Hardware

**Control Processor**
- Global coordination & control
- Routing & signalling protocols
- Build routing tables and other information needed by SPCs
- First level code server
- Reprogrammable for active processing

**Input Port Processor**

**AN Processing Element**
- APIC
- FPGA
- 32-64 MB Cache
- NB
Cell Processing
- Std. proc. for “plain” IP packets.
  - classification & routing, header processing, output queueing
- Active packets move through configured kernel plugins.
  - active function dispatcher passes packets to instances of plugin objects
  - instantiates objects or triggers download of plugin class, as needed
  - streamlined processing of SAPF packets using pre-established state
System Level Software Organization

[Diagram showing various components and their interconnections, including:
- Active Code DB
- Code Server
- Active Plugin Loader
- Plugin Requestor
- Security & Policy Controller
- Kernel
- Switch Fabric
- Processing Elements
- Control Processor
- Plugin DB
- Policy
- Rules
- Key DB
- Security Gateway
- ANN Manager
- ANTS
- Java VM
- anetd
- Policy & Signalling]

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Physical Configuration

Processor Module

Optoelectronics

Connectors

Main Circuit Board

Fiber jumper to front panel

Transmission Coder & Decoder

APIC

System FPGA
Field Programmable Port Extender

- Stackable port card
  - can be combined with PE
- Programmable hardware
  - FPGA technology
  - flexible memory config.
  - change on-the-fly
- Reprogrammable Application Device (RAD)
  - fully reprogrammable
  - four separate memory interfaces
  - memory bw: 2.4GB/s
- Network Interface Device (NID)
  - relatively static
  - adapt for different line cards

- Variety of applications
  - address lookup & packet class.
  - per flow queueing
  - traffic management
  - hardware plugins
Conclusions

- High performance active networking need not be an oxymoron.
  - Scalable systems with gigabit links and terabit throughputs are possible with current/near-term technology
  - On-going technology improvements will make AN economically viable
- Need to focus on active application development.
- Need better abstractions, tools, APIs for developers.
- Effective & open experimental platforms are essential.
  - Provide realistic testbed
  - Provide more convincing demonstrations
  - Enable system researchers and developers to build on each others efforts