CPU Scheduling for Active Processing using Feedback Deficit Round Robin

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Overview

• Scheduling for Active Networks
• Timeslicing
• Deficit Round Robin
• Feedback Mechanism
• Results
• Summary
Active Networks

Active Network Router

Execution Environment 1

Execution Environment 2

Execution Environment n

Thread Scheduler

Process Scheduler

Protocol Processing

Network
Timeslicing

- Allocates a time slice for each process
- Context switches not aligned
  => additional overhead

"context switches" due to different packet code

context switches due to scheduling
Feedback Deficit Round Robin

• Idea: align context switch with packet boundaries

"context switches" due to different packet code

context switches due to scheduling
Deficit Round Robin

- Packet-oriented scheduling for bandwidth

- Requires packet length to be known (processing time unknown in advance)
Feedback Deficit Round Robin

DRR scheduler

queue 1
  deficit
  estimate

queue 2
  deficit
  estimate

queue n
  deficit
  estimate

DRR scheduler

deficit
interrupt

processor

packet

actual processing time

adjusted deficit

adjusted estimate

estimator

packet

adjusted estimate

estimated processing time
Estimators

• Constant:
  \[ estimate_n = estimate_{n-1} = \text{const}. \]

• Exponential average:
  \[ estimate_n = \alpha \cdot actual_{n-1} + (1-\alpha) \cdot estimate_{n-1} \]

• Packet size dependent:
  \[ estimate_n = f_n(size(p_n)) \]
  \[ f_n = E(f_{n-1}, actual_{n-1}) \]
Results

![Graph showing context switches per packet vs. quantum size relative to average processing time for different FDRR settings and Timeslicing.](image-url)
Summary

Feedback Deficit Round Robin
• $O(1)$ complexity per packet
• Fairness for all queues
• Fewer context switches

Future Work:
• Evaluate different Estimators on real traffic