Gigabit Ethernet Adapter (GigE) Version 1 Architecture

William D. Richard, Ph.D.
# GigE Design Team

<table>
<thead>
<tr>
<th>Name</th>
<th>Responsibility</th>
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</tr>
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</tr>
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</tr>
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</tr>
<tr>
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<td>Physical Issues</td>
</tr>
<tr>
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<td>Wrapper/Stuff</td>
</tr>
<tr>
<td>Jon Turner</td>
<td>Beer?</td>
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</tbody>
</table>
Gigabit Ethernet Adapter (Top)
Gigabit Ethernet Adapter (Top)
Gigabit Ethernet Adapter (Top)

GBIC Guide
Gigabit Ethernet Adapter (Top)

125 MHz Osc
Gigabit Ethernet Adapter (Top)

62.5 MHz Osc
Gigabit Ethernet Adapter (Top)

XC2V1000 FPGA
Gigabit Ethernet Adapter (Top)

XC18V04 SPROM
Gigabit Ethernet Adapter (Top)

1.5V & 1.8V Regulators
Gigabit Ethernet Adapter (Top)
Gigabit Ethernet Adapter (Top)

Kludge
Gigabit Ethernet Adapter (Bottom)
Gigabit Ethernet Adapter (Bottom)

Switch Connector
Gigabit Ethernet Architecture

Gigabit Ethernet Adapter

OPP

IPP

32 bit

32 bit

32 bit

32 bit

62.5 MHz Clock

FPGA

PMC-Sierra S/UNI 2XGE

GBIC

125 MHz Clock

2

2

Fiber

or

Twisted Pair

William D. Richard- 6/19/2002 2:29 PM
GBICs

IBM FIBER GBIC

ASANTE’ TWISTED PAIR GBIC
GigE With Fiber GBIC
GigE With Twisted Pair GBIC
Gigabit Ethernet FPGA Architecture

Gigabit Ethernet FPGA

Control Cell Processor

ATM-to-Packet/Packet-to-ATM Wrappers

IP Frame Parser

IP Forward

ARP Table

ARP Request

ARP Reply

MAC Frame Parser

32

VCI=30

VCI=/=30

32

32

32

S/UNI

S/UNI CPU BUS

SW
GigE Adapter Hardware Status

- Two copies fabricated initially
- FPGA switch and MAC loopback tests ok
- 98 additional copies in process at fab house
- Software simulation completed and tested
- FPGA VHDL coding underway
- Delivery to kits groups expected ____
- Each kits group should receive ____