Network Statistics Module

- Counts the number of times that events occurs
  - Track a large number (256) of events, not just one
  - Maintain a long (32-bit) counts that won’t wrap between counter reads

- Key observation:
  - Random Access Memory (RAM) much more abundant than Flops

- Key concept:
  - Time-multiplex RAM to reduce the number of flops needed to store count states
## Operation of the Statistics Counter

- **Event_1_number**
  - Identifies which of the 256 counters to use
- **Inc_event_1**
  - Adds 1 to the counter [event_1_number]
- **Cntr_read**:
  - Reads the 32-bit value of the counter (cntr_data) when data_strobe issued for Counter [event_1_number]
  - Output valid when data_strobe goes high

## Memory Options for FPGA Circuits

- **FPGA circuits often use:**
  - On Chip RAM
  - Off Chip SRAM or DRAM

Diagram from: Xilinx, Inc.
Memory Configurations

Virtex On-Chip SelectRAM™ Memory Hierarchy

- DSP Coefficients
- Small FIFOs
- Shallow/Wide

- Distributed RAM
  - 16 x 1 bytes

- Block RAM
  - 4K x 1
  - 2K x 2
  - 1K x 4
  - 512 x 8
  - 256 x 16 kilobytes

- Large FIFOs
- Packet Buffers
- Video Line Buffers
- Cache Tag Memory
- Deep/Wide

- SDRAM
- ZBT
- SSRAM
- SGRAM
- DDR
- QDR

External RAM
- megabytes

Terabit Memory Continuum

Highest performance FPGA memory system

Virtex BlockRAM

- CLK{A,B}
  - Independent
- EN{A,B}: Enable
  - (1=enable)
- WE{A,B}: Write enable
  - (0=read, 1=write)
- RST{A,B}: Reset output bus
  - Output=0, content unchanged
- ADDR{A,B}[:#]: Address
- DI{A,B}[:#]: Data In
- DO{A,B}[:#]: Data Out

Diagram from: Xilinx, Inc.
On-Chip, Dual-port Block RAM

- Contains 4096 bits of data (256 x 16)
- Each port (a/b) can be read independently
  - Address (addrA, addrB)
  - Data (DataA, DataB)
  - Read Enable (ena, enb)
  - Write Enable (weB)
  - Clock (clka, clkb)

Timing of the Block RAM

- Read from Memory[addrA] when enA active
  - Result available 1 cycle later
  - Except when other port is writing to the same location
- Write to Memory[addrB] when enB and weB active
  - Value of DinB loaded into memory