CSE 535: Lecture 3

Synthesis, Placement, and Routing of Reconfigurable Hardware

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http://www.arl.wustl.edu/arl/projects/fpx/cse535/

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Logical

<table>
<thead>
<tr>
<th>x</th>
<th>F</th>
<th>x y</th>
<th>y</th>
<th>x y'</th>
<th>F = x'</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0 0</td>
<td>1</td>
<td>0 0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0 1</td>
<td>1</td>
<td>1 0</td>
<td>0</td>
</tr>
</tbody>
</table>

Driver

F = x

AND

F = x y

OR

F = x + y

XOR

F = x ⊕ y

NAND

F = (x y)'

NOR

F = (x + y)'

XNOR

F = x \& y

Slide From: Embedded Systems Design: A Unified Hardware/Software Introduction, (c) 2000 Vahid/Givargis
Random Access memory (RAM)

- **Volatile memory**
  - Bits are not held without power supply

- **Addressing Data**
  - A word consists of several memory cells, each storing 1 bit
  - rd/wr when row is enabled by decoder, each cell has logic that stores input data bit when rd/wr indicates write or outputs stored bit when rd/wr indicates read

Technology-Dependent Logic: FPGA

- Circuits mapped into physical circuits
  - Field Programmable Gate Arrays (FPGAs)
    - LookUp Table (LUT)
  - Memory Element, Addressed by inputs
Field Programmable Gate Arrays: CLB

- **Look Up Table (LUT) Function Generator**
  - Calculates arbitrary \( F(f_1,f_2,f_3,f_4) \)

- **Soft Interconnect**
  - Propagates signals

- **State Storage**
  - Bistable latch
  - Edge-triggered \( F/F \)

- **Efficiency**
  - ~10x performance hit over full-custom logic
  - Latest Silicon technology (.25um)

Field Programmable Gate Arrays: Virtex

- Diagram From: Xilinx, Inc (Courtesy Peter Alfke)
Closer View (Wrapper_App’s State Machine)

- Each block represents one SLICE

Placement Algorithms

- Simulated Annealing
  - Name comes from analogous physical process of heating and then slowly cooling a substance to obtain a strong crystalline structure
  - At high temperatures, atoms can move freely
  - At lower temperatures, elements lock in place
  - Thermal Equilibrium at each temperature

- Algorithm
  - Start with Randomly-placed gates on IC
  - Sum the weight (Length) of Interconnect
  - Randomly swap the location of components
  - Keep placements that have lower weights
### Unconstrained Layout

- Actual layout of SOC Firewall on VirtexE-2000 FPGA.
  - Color regions correspond to used resources
  - Vertical stripes correspond to Block RAMs

### Unconstrained Layout for Related Logic

- Overall placement random, but
- Components connected to each other will tend to be placed together
Placement and Routing Delay

- Wires have finite resistance (R)
- Wires have finite capacitance (C)
- \( T = RC \) Delay required to transport a signal

Vector-based Interconnect

The circles show 1.4-ns routing delay

Programmable Interconnect Points (PIPs)

- Routing interconnect implemented with pass gates
- Delay is added with additional PIPs
Complete Hardware Design Flow

1. Compile circuit (vcom)
2. Verify Functionality (vsim)
3. Place and Route with constraints (Xilinx)
4. Synthesize Logic to Xilinx gate technology (Synplicity)
5. Verify valid data processing
6. Test Module with actual traffic input
7. Upload bitfile To FPX for testing
8. Verify Post Place & Route Timing (ModelSim)
9. Generate bitstream (Xilinx)
10. Constrain Placement to FPX RAD
11. Generate bitstream (Xilinx)
12. Verify Post Place & Route Timing (ModelSim)
13. Test Module with actual traffic input
14. Upload bitfile To FPX for testing
15. Verify valid data processing
16. Compile circuit (vcom)