WIPRO
Applying Thought

System-on-Chip Designs

Strategy for Success

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Conventionally, ASIC design involved development of medium complexity Integrated Circuits (of less than 500,000 gates). These had a cycle time of roughly 6 months, were processed with 0.35u technology, and were essentially made up of core logic and some hard macros, like on-chip SRAMs.

With rapid advances in semiconductor processing technologies, the density of gates on the die increased in line with what Moore's law predicted. This helped in the realization of more complicated designs on the same IC. Over the last few years, with the advent of bleeding edge technology applications like HDTV and 3rd generation mobile devices, an increasingly evident need has been that of incorporating the traditional microprocessor, memories and peripherals - or in other words the whole system - on a single silicon. This is what has marked the beginning of the SoC era.

Research agency In-Stat predicts robust market growth for SoCs, estimating that volumes will increase an average of 31% a year. Paradoxically today, the emergence of system-on-chip technology has brought with it a whole spectrum of opportunities and challenges. Opportunities come in the form of drastic reduction in the overall cycle time of the system with superior performance levels; challenges are the result of deep sub-micron complexities, testability issues and time-to-market pressures.

This paper attempts to confront these opportunities and challenges, and evolve a strategy that can successfully realize an SoC from concept to silicon. The five key aspects of a successful design strategy discussed here are - *Architectural strategy, Validation strategy, DFT Strategy, Synthesis & Backend strategy, and Integration strategy.*

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System-on-chip

System-on-chip has been a nebulous term, that mystically holds out a lot of excitement, and has been gaining momentum in the electronics industry. While the potential is huge, the complexities are several, and countering these to offer successful designs is a true engineering challenge.

Witness these market trends:

- Research agency In-Stat predicts robust market growth for System-on-Chips (SoCs), estimating that volumes will increase an average of 31% a year, reaching 1.3 billion units in 2004.
- SoCs make up 20% of chip market today, this will be 40% in 2004.
- Semiconductor Companies are investing two-thirds of their R&D resources in the System-on-Chip arena.

These trends are ample evidence that SoCs are growing in importance in the semiconductor industry. The reasons are not far to look: SoCs make available, on a single piece of silicon, the embedded IP and high system-level integration required for performance demanding applications today. This enables semiconductor manufacturers to cost-effectively meet specific system requirements while delivering competitive time-to-market advantage.

Paradoxically, if the opportunities look promising, the challenges are no less daunting. While opportunities come in the form of drastic reduction in the overall cycle time of the system with superior performance levels, challenges are in the form of deep sub-micron complexities, faster timing closure requirements, verification challenges and the need for an extensive portfolio for pre-verified IP components.

How then does one adopt efficient methodologies and processes, and what are the strategies of effective SoC designs? At Wipro Technologies, we translated a decade of ASIC and VLSI design experience into a proven design methodology flow for complex SoCs.

SoC designs typically exhort several man-hours of skilled engineering resources. In catering to a competitive market with shortened product cycle times, it is important to offer tangible reductions in design cycle time. Two key aspects help Wipro attain time-to-market advantage, our biggest customer promise. The first is a virtual Verilog world called the SoC-RaPTor that provides an architectural framework for quickly defining and designing SoCs. The second is a conscious effort to build a design suite of reusable IP components.

Five years ago, Wipro laid down a set of guidelines and a hygiene code to force consistent IP design processes that emphasizes robustness of implementation, thoroughness in verification and modularity and configurability in design. A significant measure of the reuse component of Wipro's IPs is the high scores they attain on the Synopsys-Mentor Graphics OpenMORE Reuse Methodology Scale. Today, Wipro has built itself a library of IPs that embraces the networking, wireless and consumer multimedia domains. These IPs shrink our SoC cycle time significantly, as they are pre-verified and developed with reuse in mind.

Despite such enablers, SoC design and validation demands certain measured approaches. Following are what we call the Five Guiding Principles of SoC design.

1. Architecture Strategy

A key dependency that actually defines an SoC architecture is the kind of processor that one uses as the central processing element. At Wipro, significant focus has been on the ARM processor technology, since we believe that will drive the evolving market for embedded applications, mobile devices and next generation information appliances. Our expertise with ARM cores and technology is also a derivative of our long standing association with ARM, and our status as an approved ARM Design Center.

The SoC's target application demands may necessitate the inclusion of DSP cores in the design consideration. Another design aspect to be thought through is the kind of processor and system BUS that is to be implemented within the system. The use of standard buses like AMBA AHB (Advanced High Performance bus) and APB (Advanced peripheral bus) is definitely advantageous vis-a-vis the use of proprietary buses. With standard buses, the integration task of putting together the SoC becomes easier, especially if the IP cores that are available support the chosen standard bus protocol.

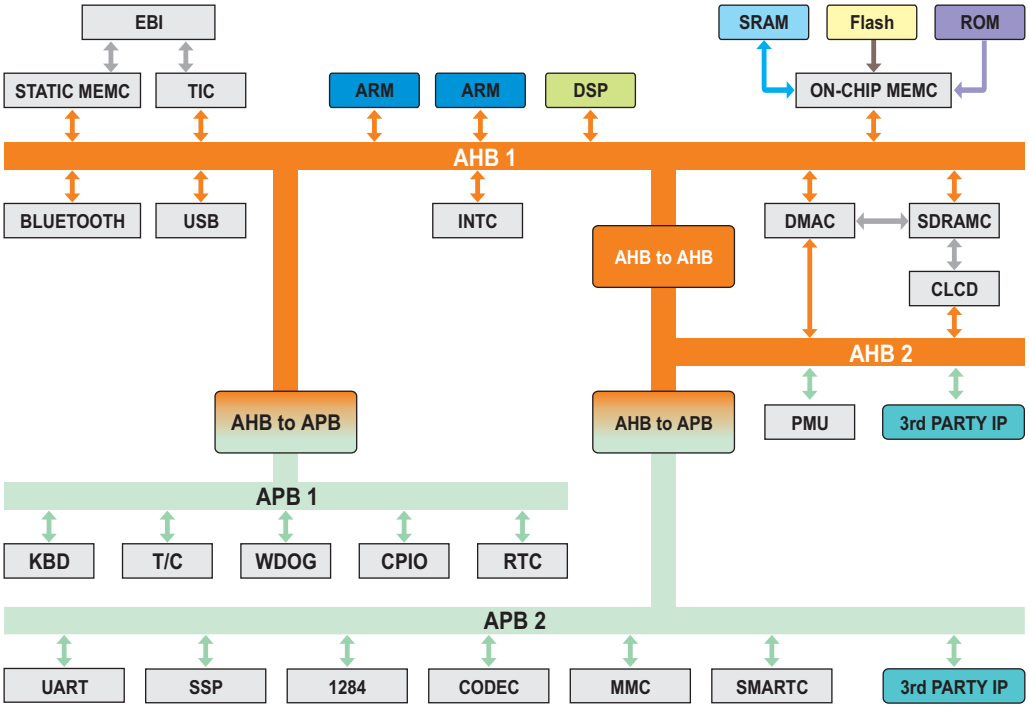

Figure 1: Wipro's SoC-RaPTor Platform

Wipro's SoC-RaPTor platform is built with architecture specific component blocks like DMA controllers, Interrupt controllers, Arbiters, Decoders and Memory controllers, as well as Application specific IPs such as Bluetooth, 802.11, CAN controllers USB, 1394, Ethernet, etc. Several of these IPs are available with an optional ARM interface, thus facilitating easy plug and play into the SoC design.

Two key design-for-integration techniques are required to address the challenges in integrating the IpP cores into a SoC.

a) Parameterization, which is a key technique for customizing soft cores by using generics or parameters. With the help of this, one can select or eliminate commonly customized features during synthesis like the number of DMA channels in a DMA controller, the number of flash banks in a Flash controller, and so on.

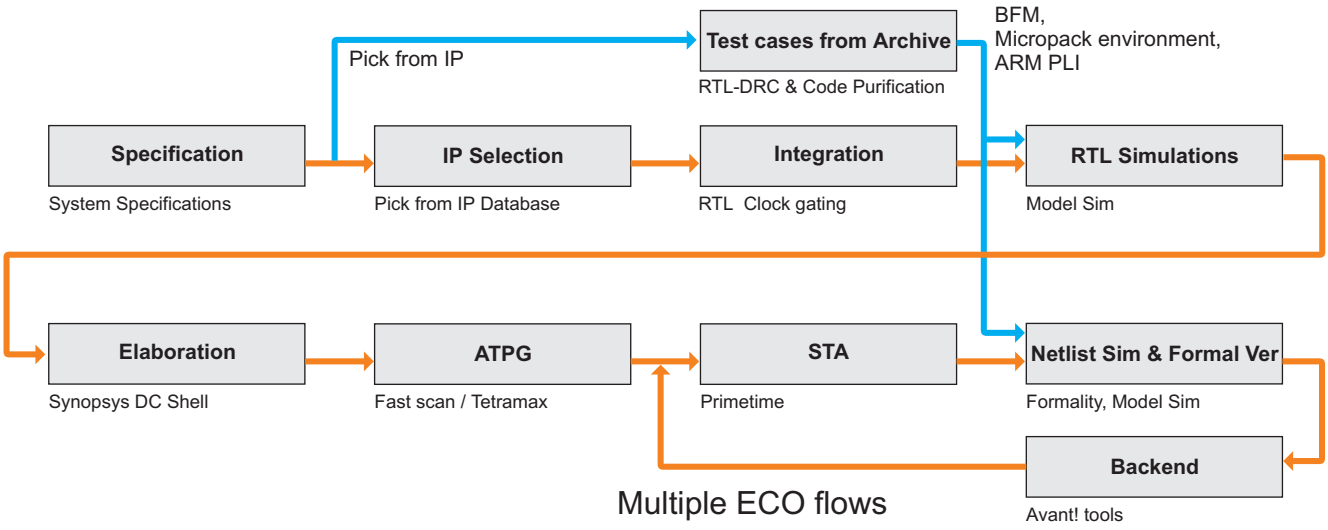

Figure 2: A typical SoC front-end flow

b) Functional partitioning, where use of multiple hard, firm and soft cores is made instead of single monolithic hard cores to eliminate routing problems when the SoC is laid out on silicon. Timing critical components like the CPUs or function critical analog components are usually implemented as hard macros. Functions without any critical timing requirements but which require Intellectual property (IP) encryption fall under the definition of Firm macros. Finally the Functions which require no fixed layout or IP encryption and those which are frequently custpomized are called soft cores.

2. Design-for-Test Strategy

Because verification forms such a crucial aspect of SoC designs, and since manufacturing defects are a no-compromise zone, Wipro's SoC flow mandates Design for Test (DFT). In this strategy, most common physical defects are modelled as faults and necessary circuits are included in the design to facilitate checking for these faults. These methodologies and automated processes that insert logic in order to increase the design testability form the essence of DFT.

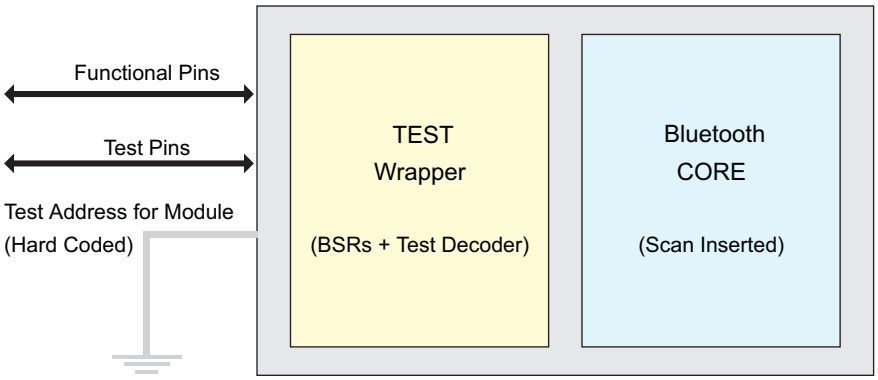

Figure 3: Module level scan methodology

DFT is implemented using a full scan, muxed flip-flop style of scan insertion. Almost every node in the design is made controllable and observable. Multiple Scan chains are employed, one in each of the modules and these scan chains are stitched at the SoC Device level.

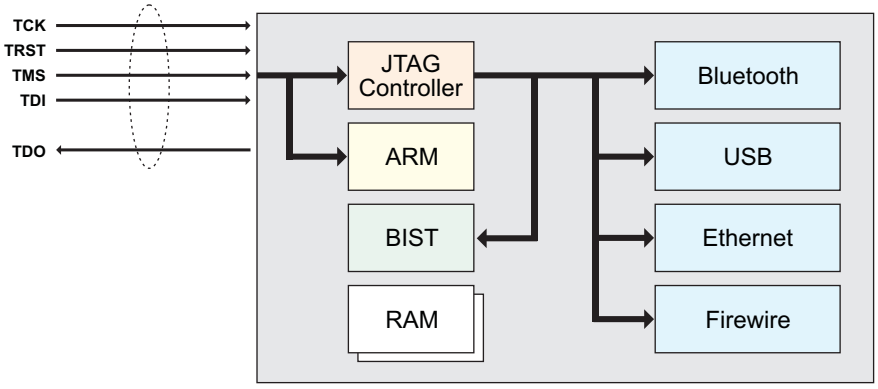

Figure 4: Device level scan methodology

For embedded memories, Built in Self-Test (BIST) and Module Test are best used. BIST uses random pattern generator and compare logic, which are already placed inside the chip. The address and data patterns are generated and loaded into the memory and the locations are read back and compared by the comparator, which flags error if there are any discrepancies. In module test, the chip level I/O pins are used with the help of multiplexers to load and observe the patterns and an external logic is used to generate and compare.

3. Validation Strategy

When several varied functions assemble on a single piece of silicon, verification can become an arduous activity. At Wipro, we follow a "Verify Early" strategy. The verification progresses as the SoC unfolds i.e., at every level of the design flow - RTL, gate level and post layout gate level with timing. As much as 60% of the SoC development time is spent on verification. A high level of code coverage is mandated to determine that the design conforms to the specifications. Also, it is important to cover module testing as exhaustively as system testing is covered.

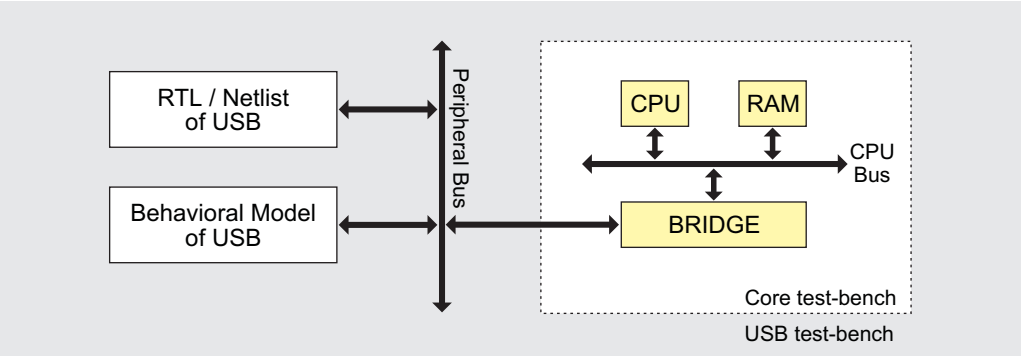

Figure 5: Module level validation set-up

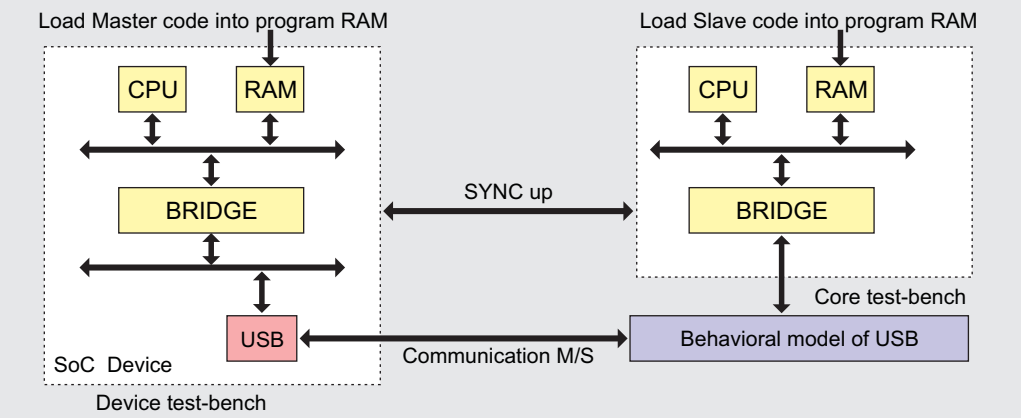

Figure 6: Device level validation set-up

There are two issues to be considered when it comes to validating the SoC. First, we need to verify the IP cores thoroughly. Secondly, we need to verify their integration in the system. To meet the first requirement, IP cores, which are designed and developed at Wipro, are subjected to extensive IP validation suites that include test benches and behavioral models. The IP's overall functionality is exhaustively verified thus, and the module level verification is effectively translated to the SoC device level by integrating the same test cases in the Test Bench.

In order to verify the integration of IP blocks, a separate set of integration test vectors are created, based on typical scenarios. Code coverage and functional coverage tools are employed to trim the test vector set.

4. Synthesis and Backend Strategy

As Silicon processing moves into deep sub micron dimensions, physical effects become more prominent. Some of the common effects are Electromigration, IR drop, Cross Talk, 3D noise, antenna effects and EMI effects. As a result interconnect delays, power, signal integrity, manufacturability, reliability all become prime objectives along with area and gate delays.

Tackling these myriad issues requires chip planning, DFT planning, clocks planning, power planning and timing and area budgeting at a very early stage of the design cycle. This, then is the core of Wipro's Backend strategy.

The four-week SoC development cycle time, requires an early timing closure. Traditionally, for process geometries as low as 0.35u, standard logic synthesis was considered effective in synthesizing a large ASIC. With the transition to deep sub-micron geometries, painful multiple iterations are required to ensure performance. As it were, the front-end designer creates a netlist with limited concept of the physical world and hence performance/area tradeoffs are made with incomplete data. On the other hand the backend engineer has no idea of the designer's intent and hence "Flow creation" becomes more important than design.

At Wipro, this was a constant realization and finally a conscious effort had to be made to eliminate the "Wall", and ensure front end logic design and backend flow operate seamlessly. The answer was in implementing physical synthesis instead of logic synthesis.

Physical Synthesis flow diagram on the following page . . .

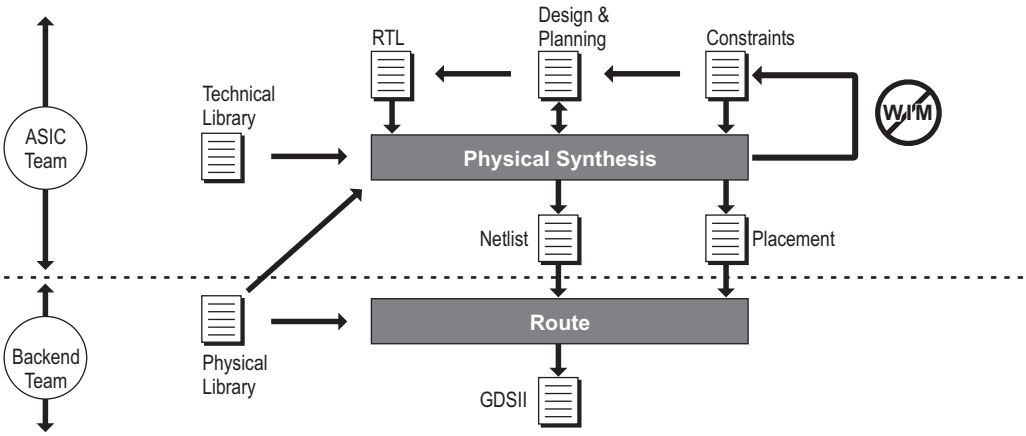

Figure 7: Physical Synthesis flow

What the physical synthesis flow achieved was to bring physical domain in the form of placement, obstructions, congestion, power and routing into the logical synthesis world. Currently, Wipro engineering is experimenting with another methodology of placement optimizations based on constraints, to improve the timing closure cycle. This is called the single pass flow.

5. Integration Strategy

Ultimately, all of the above aspects have to be coherently assembled to instal a smooth spin-off flow strategy. This calls for automating the entire SoC Design Cycle in the form of scripts. Beginning with the SOC directory structure creation, extraction of the IP Cores and their validation files, creation of the device top Source file, Simulation, synthesis and ATPG generation, right up to signoff - the whole activity can be automated.

Such an automation mechanism is to be a key feature of Wipro's SoC-RaPTor platform. The benefit, we expect, will be a definite increase in the speed and reliability of the SoC design spin-off, and a reduction in engineering resource that have to be deployed for a typical SoC spin-off. More importantly, this will help our customers realize their products faster.

Conclusion

Architecture design, IP selection, integration, validation and Physical synthesis form the cornerstones of the SoC design process. The five strategies described above will, we believe, give the much needed reliability, improved performance and reduced overall system cost necessary for today's product companies to roll out high performance systems faster and better than ever before.

References

Synopsys Physical Synthesis: The Solution for Timing Closure by *Toovit Begun*, Synopsys Inc.

About the Authors

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If you need to contact us regarding any clarification or feedback, mail us at SoC@wipro.com

About Wipro

Wipro Technologies is a part of Wipro Limited (NYSE: WIT), and is a leading global provider of high end IT solutions. The IT solutions provided include application development services to corporate enterprises and hardware and software design services to technology companies. The company's top clients include Lucent, Canon, Epson, Hitachi, Sony, Toshiba, Lucent, Cisco, IBM and ARM.

Wipro in Embedded Technologies

Wipro Technologies offers industry leading skills in embedded design services. The spectrum of offerings covers embedded software, along with expertise in concept-to-silicon services for ASIC and SoC designs as well as complex, high-frequency FPGA/Board designs. Our well-grounded design methodology and tools flow is complemented by strategic design partnerships with industry leading companies like ARM, Artisan, Symbian, and TSMC.

As an approved ARM Design House, Wipro's ARM knowhow spawns the spectrum of design through implementation and testing, all the way to intensive physical design and silicon validation. Wipro's value proposition stems from its ability to leverage on its extensive intellectual property (IP) portfolio, and systems knowledge, to offer early-to-market, high-performance, SoCdesigns, with best chances of first time silicon success

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