CS/EE 260 – Exam 1

Spring 2000

No books, no notes, no calculators. Write in the spaces provided. Be neat.

1. (5 points) What is the binary representation of 678? What is the octal representation? Hexadecimal?

\[
\begin{align*}
678 &= 512 + 166 \quad 2^9 \\
166 &= 128 + 38 \quad 2^7 \\
38 &= 32 + 6 \quad 2^5 \\
6 &= 4 + 2 \quad 2^2 \\
2 &= 2 + 0 \quad 2^1
\end{align*}
\]

So, \(678 = 1010100110_2 = 1246_8 = 2a6_{16} \).

2. (5 points) Use a Karnaugh map to find the simplest possible expression for \(F(A,B,C,D)=\Sigma_m(0,1,2,5,6,7), \ d(A,B,C,D)=\Sigma_m(8,10,12,13,15)\).

\[
\begin{array}{cccc}
CD & & & \\
00 & 01 & 11 & 10 \\
00 & 1 & 1 & 0 & 1 \\
01 & 0 & 1 & 1 & 1 \\
11 & x & x & x & 0 \\
10 & x & 0 & 0 & x \\
\end{array}
\]

\[F = A'B'C' + A'CD' + BD\]
3. (5 points) Draw a schematic for a circuit that directly implements the logic function \( A + B' C + (A(B+C')) \).

\[
\begin{align*}
A + B' C + (A(B+C')) &= A(1+B+C') + B'C = A + B' C
\end{align*}
\]

Simplify the logic expression and draw a schematic for the circuit that implements the simplified expression.

4. (5 points) Consider the Karnaugh map shown below. How many terms are there in the simplest sum-of-products expression for this Karnaugh map? Is there any four input logic function that requires more terms? Why or why not?

There are eight terms in the simplest sum of products expression, since none of the eight minterms can be combined with other minterms.

There is no four input logic function that requires more terms. Any logic function with fewer than eight minterms obviously requires fewer terms in the simplest sum of products expression. In any logic function with more than eight minterms, you can combine some minterms into common terms, resulting in no more than eight altogether.
5. (5 points) Consider the circuit shown below. If this were implemented using CMOS technology, how many transistors would be required?

Each AND and OR gate requires 6 transistors, each NAND and NOR requires 4 and each inverter requires 2, so the total is 28.

6. (5 points) The timing diagram shown below shows the output of the two circuits shown, when their inputs change from 1 to 0. All the inverters in the circuits are identical. Label the waveform that corresponds to circuit A, assuming that both circuits are implemented in CMOS. Explain why your choice is correct.

The lower curve of the pair corresponds to circuit A. The reason is that in circuit A, there is just one inverter and hence one pullup transistor. There are two in B and when the pullups are enabled they act as resistances. The resistance in B is half as large as the resistance in A (since there are two equal resistances in parallel). So, the voltage at the output rises faster in circuit B than in circuit A.

7. (5 points) What bit pattern is used to represent –11 in 2s complement notation in a computer that uses 5 bit words? What bit pattern would be used in 1s complement? Sign-magnitude?

+11 = 01011, so in 1s complement –11=10100, in 2s complement –11=10101, and in sign-magnitude –11 = 11011.
8. (15 points) In the circuit shown below output $d_i$ is the odd function computed over inputs $a_0, a_1, \ldots, a_i$. If each exclusive-or gate has a propagation delay of 1 ns, what is the worst-case delay in this circuit (the time from when some input changes to latest time that some output changes)? Show a logically equivalent circuit using only exclusive-or gates that has a worst-case delay of 3 ns.

The worst-case delay for this circuit is 7 ns. Changes in $a_0$ and $a_1$ can affect $d_i$ after 7 ns, but changes to other inputs will cause changes to outputs after less than 7 ns.
9. (10 points) Write a VHDL specification for a circuit with inputs $A,B,C,D$ and outputs $X = ABC' + A(C+B'D')$ and $Y = (B+C')(A'+D)$.

```vhdl
library IEEE;
use IEEE.std_logic_1164.all;
entity foo is
  port(A,B,C,D: in std_logic; X,Y: out std_logic);
end foo;

architecture dataflow of foo is
begin
  X <= (A and B and (not C)) or (A and (C or ((not B) and (not D))));
  Y <= (B or (not C)) and ((not A or D));
end dataflow;
```

10. (5 points) Consider the sequential circuit shown below. Fill in the waveform for output $Z$ in the timing diagram. Assume $Z=0$ initially.

![Equivalent circuit](image-url)

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