1. (10 points) Several flip flops and latches are shown below. Identify each one completely (e.g. Master-Slave SR flip flop) and label the inputs and outputs in the “usual” way.
2. (10 points) Give the next-state equations and the state table corresponding to the sequential circuit shown below.
3. (20 points) Complete the VHDL program shown below so that it implements the state diagram.

```vhdl
library IEEE;
use IEEE.std_logic_1164.all;

entity foo is
  port (
    a, clk: in STD_LOGIC;
    x, y: out STD_LOGIC
  );
end foo;

architecture bar of foo is
  type state_type is (apple, peach, squash, pit);
  signal state: state_type;
begin
  process(clk) begin
    if clk'event and clk = '1' then
      signal state: state_type;
    end process;
    x <= '1' when '1' when '0';
    y <= '1' when '0';
end if;
end process;
```

```vhdl
1/00
a/xy

apple

peach

0/00
1/01
1/00

squash

pit

1/10
0/11
0/01
1/01
```

```vhdl
end foo;
architecture bar of foo is
  type state_type is (apple, peach, squash, pit);
  signal state: state_type;
begin
  process(clk) begin
    if clk'event and clk = '1' then
      signal state: state_type;
    end process;
    x <= '1' when '1' when '0';
    y <= '1' when '0';
end if;
end process;
```

```vhdl
end architecture bar of foo;
```
4. (20 points) Consider the circuit shown below. Assume that each gate has a maximum propagation delay of 2 ns, that clock skew in the circuit is 1 ns and that the flip flop setup time constraint is 2 ns and that its propagation delay is 3 ns. What is the maximum clock frequency for which the circuit can be operated without violating the setup time constraint (consider only the circuit path between the two flip flops)? Show how to modify the circuit so that it can operate with a clock frequency of 100 MHz (you may use gates with more than two inputs and you may assume that they have the same propagation delay as the two input gates).
5. (10 points) Consider the circuit shown below. Assuming all the inverters are identical, and that signal X changes as indicated on the timing diagram, which of the other two curves corresponds to signal A and which to B (indicate your answer by labeling the curves appropriately). Explain your answer.

6. (10 points) Consider an SRAM with 32K words of 32 bits each. How many bits of memory does the SRAM contain (approximately)?

How many address signals are needed to address all the words in the SRAM?

Assuming a square memory array (same number of rows and columns) and that the SRAM uses the standard coincident decoding method, how many address signals are input to the row decoder?
7. (15 points) The circuit shown below implements a “universal” counter that will count in an arbitrary order. What values for the inputs \( \text{next}_0, \ldots, \text{next}_7 \) will cause the counter to implement the Gray code sequence 000, 001, 011, 010, 110, 111, 101, 100? Write the values next to the wires in the blank spaces given.
8. (15 points) Consider the PLA shown below. What logic equations does it implement, in the configuration shown?

Can the following set of logic equations be implemented using this PLA?

\[
A = UV' + W'X + VX \\
B = U'WX + W'X + UX'
\]

Why or why not?