1. (10 points) Several flip flops and latches are shown below. Identify each one completely (e.g. Master-Slave SR flip flop) and label the inputs and outputs in the "usual" way.

- **JK Master Slave Flip Flop**
- **SR Latch**
- **D Latch with Enable**
- **Positive Edge-Triggered D Flip Flop**
2. (10 points) Give the next-state equations and the state table corresponding to the sequential circuit shown below.

\[ D_U = UA + V \quad D_V = UV' A' \]

<table>
<thead>
<tr>
<th>UV A</th>
<th>D_U</th>
<th>D_V</th>
<th>X</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
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<tr>
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<td>1</td>
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<tr>
<td>11</td>
<td>1</td>
<td>0</td>
<td>0</td>
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</tbody>
</table>
library IEEE;
use IEEE.std_logic_1164.all;

design entity foo is
   port (a, clk: in STD_LOGIC;
       x, y: out STD_LOGIC
   );
end foo;

architecture bar of foo is
   type state_type is (apple, peach, squash, pit);
   signal state: state_type;
begin
   process(clk) begin
      if clk'event and clk = '1' then
         if state = apple and a = 0 then
            state <= peach;
         elsif state = peach and a = 0 then
            state <= pit;
         elsif state = peach and a = 1 then
            state <= squash;
         elsif state = pit and a = 0 then
            state <= squash;
         elsif state = squash and a = 0 then
            state <= peach;
         elsif state = squash and a = 1 then
            state <= apple;
         end if;
      end if;
   end process;

   x <= '1' when (state = squash and a = 1) 
      or (state = pit and a = 0) else '0';
   y <= '1' when state = peach OR state = pit else '0';
end bar;
4. (20 points) Consider the circuit shown below. Assume that each gate has a maximum propagation delay of 2 ns, that clock skew in the circuit is 1 ns and that the flip flop setup time constraint is 2 ns and that its propagation delay is 3 ns. What is the maximum clock frequency for which the circuit can be operated without violating the setup time constraint (consider only the circuit path between the two flip flops)? Show how to modify the circuit so that it can operate with a clock frequency of 100 MHz (you may use gates with more than two inputs and you may assume that they have the same propagation delay as the two input gates).

The sum of setup, clock skew and the propagation delays is 14 ns, so the maximum frequency is about 71 MHz.

To make the circuit run at 100 MHz, replace the combinational circuit with a two level circuit. The input to the second flip flop is

\[(A+C) \cdot (B+C(Y+Q)) = AB + ACY + ACQ + BC\]

So, we can modify the circuit as shown below to reduce the propagation delay by 4 ns, making 100 MHz operation possible.
5. (10 points) Consider the circuit shown below. Assuming all the inverters are identical, and that signal $X$ changes as indicated on the timing diagram, which of the other two curves corresponds to signal $A$ and which to $B$ (indicate your answer by labeling the curves appropriately). Explain your answer.

The top inverter at left is driving 4 other inverters, so it has a larger capacitance to charge than the bottom inverter does. This makes it slower.

6. (10 points) Consider an SRAM with 32K words of 32 bits each. How many bits of memory does the SRAM contain (approximately)?

- about 1 million bits ($2^{20}$ to be more precise)

How many address signals are needed to address all the words in the SRAM?

- 15 since $32K = 32,768 = 2^{15}$

Assuming a square memory array (same number of rows and columns) and that the SRAM uses the standard coincident decoding method, how many address signals are input to the row decoder?

- The array has 1024 rows and 1024 columns, so the row decoder uses 10 address bits.
7. (15 points) The circuit shown below implements a “universal” counter that will count in an arbitrary order. What values for the inputs $next_0$, . . . , $next_7$ will cause the counter to implement the Gray code sequence 000, 001, 011, 010, 110, 111, 101, 100? Write the values next to the wires in the blank spaces given.
8. (15 points) Consider the PLA shown below. What logic equations does it implement, in the configuration shown?

\[ A = U V W' + W'X + U V' X \]
\[ B = U W' X' + U V' X \]

Can the following set of logic equations be implemented using this PLA?

\[ A = U V' + W'X + V X \]
\[ B = U' W X + W'X + U X' \]

Why or why not?

No, it cannot. This set of equations has five distinct products, but the PLA has only four AND gates, so it can only form four products.