1. (10 points) Draw a state diagram corresponding to the VHDL module shown below. Is this
VHDL for a Mealy model circuit or a Moore model circuit? What is the minimum number of
flip flops needed in a circuit implementing this VHDL module?

library IEEE;
use IEEE.std_logic_1164.all;
entity partB is
  port (A, B: in STD_LOGIC;
        X, Y: out STD_LOGIC);
end partB;
architecture explicit of partB is
  type state_type is (red, blue, yellow);
  signal state: state_type;
begin
  process(clk) begin
    if clk'event and clk = '1' then
      if state = red and B = '0' then
        state <= yellow;
      elsif state = red and A = '1' and B = '1' then
        state <= blue;
      elsif state = blue and A = '0' then
        state <= yellow;
      elsif state = yellow and A = '0' and B = '0' then
        state <= blue;
      elsif state = yellow and A = '1' and B = '1' then
        state <= red;
      end if;
    end if;
  end process;
  X <= '1' when state = red else '0';
  Y <= '1' when state = yellow and A /= B else '0';
end explicit;