1. (6 points) List all the minterms for the expression \((B' + A)C + AC' + BC\).

List the maxterms for the expression.
2. (5 points) Show that the following Boolean equation is true using algebraic simplification (not Karnaugh maps). Show your work.

\[ AB + BC' + CD = (B + C)(B + D)(A + C' + D) \]
3. (8 points) The attached simulation output is from an execution of the simple processor introduced in section 1 of the lecture notes. The instruction set for the processor appears below. Answer the following questions using the simulation output.

What does the instruction stored at location 000C do?

What is the value of memory location 0011 at time 6 µs?

What is the value of the program counter at time 4450 ns?

What is the value of memory location 0010 at time 7 µs?

0000  halt execution
0001  negate the value in the ACC
1xxx  change the value of the ACC to xxx
2xxx  load the contents of memory location xxx into the ACC
3xxx  load the ACC from the memory location whose address is stored in memory location xxx
4xxx  store the value in the ACC in memory location xxx
5xxx  store the value in the ACC in the memory location whose address is stored in memory location xxx
6xxx  change the value of the PC to xxx
7xxx  change the value of the PC to xxx if ACC = 0
8xxx  change the value of the PC to xxx if ACC > 0
9xxx  change the value of the PC to xxx if ACC < 0
axxx  add the value in memory location xxx to the ACC
4. (10 points) Draw a logic circuit using the smallest possible number of simple gates (AND, OR and inverters, only) for the logic expression \(UX' + X(V + Z') + (V' + U)X'Z'.\)

How many transistors are required by a CMOS version of this circuit (that uses just and-gates, or-gates and inverters)? Show how to improve it by using NAND and NOR gates. How many transistors does this version require?
5. (8 points) Use a Karnaugh map to find the simplest **sum-of-products** expression for
\[ F(X,Y,Z) = \Sigma m(1,2,4), \quad d(X,Y,Z) = \Sigma m(3,6) \]

Use a Karnaugh map to find the simplest **product-of-sums** expression for
\[ F(A,B,C,D) = \Sigma m(1,2,6,7,8,9,15), \quad d(A,B,C,D) = \Sigma m(3,4,5,11) \]
6. (5 points) Show how to implement the function $F(A, B, C, D) = \Sigma m(0, 2, 5, 7, 8, 9, 11), \ d(A, B, C, D) = \Sigma m(3, 4, 6, 15)$ using an 8 input multiplexor.
7. (10 points) The circuit below shows a combinational circuit that implements a 5 bit version of the parallel pulse-parity function from design problem 2. What is the worst-case propagation delay for a 64 bit version of this circuit, using only simple gates with a delay of 1 ns? (The worst-case propagation delay is the maximum time from when an input changes until all outputs reach their final value.)

![Circuit Diagram]

The circuit outlined below is a lookahead version of the same circuit. The boxes represent a repeated sub-circuit. In the rightmost box, fill in this circuit. What is the worst-case delay for a 64 bit version of this circuit, implemented using simple gates?

![Lookahead Circuit Diagram]
8. (15 points) The circuit shown at left below implements a ternary (base 3) half-adder. The pair of input bits \((A_i, B_i)\) represents a single ternary digit (the bit pair 00 represents the ternary digit 0, the bit pair 01 represents the ternary digit 1 and the bit pair 10 represents the ternary digit 2). Similarly for the outputs \((X_i, Y_i)\). We can build a ternary increment circuit by combining these ternary half-adder circuits together, as shown at right below. Suppose that the input presented to a ternary increment circuit with four ternary digits corresponds to the ternary value 1022 and that the carry into the least-significant bit is high. What are the values of the nine output bits? Fill in your answer below the output signals listed below.

\[
\begin{align*}
&C_{\text{in}} \\
&A_0 \rightarrow X_0 \\
&B_0 \rightarrow Y_0 \\
&A_1 \rightarrow X_1 \\
&B_1 \rightarrow Y_1 \\
&A_2 \rightarrow X_2 \\
&B_2 \rightarrow Y_2 \\
&A_3 \rightarrow X_3 \\
&B_3 \rightarrow Y_3 \\
&C_3 = C_{\text{out}}
\end{align*}
\]
The partial VHDL module below implements a ternary increment circuit with 8 ternary digits. Complete the missing parts. Your VHDL should be complete and syntactically correct.

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity ternaryInc is
    Port (A, B : in std_logic_vector(7 downto 0);
          Cin : in std_logic;
          X, Y : out std_logic_vector(7 downto 0);
          Cout : out std_logic);
end ternaryInc;

architecture arch1 of ternaryInc is
    signal C: std_logic_vector(7 downto 0);
begin
    process(A, B, Cin, C) begin
        ...
    end process;
end arch1;
```
9. (10 points) The figure shown below is a state diagram for a sequential circuit with one input $A$ and two outputs $X$ and $Y$. Is this a Moore model circuit or a Mealy model circuit? Fill in the values in the next state table.

<table>
<thead>
<tr>
<th>$S_1S_0A$</th>
<th>XY</th>
<th>$D_1D_0$</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>00</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>01</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>01</td>
<td>1</td>
<td></td>
</tr>
<tr>
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<td></td>
</tr>
<tr>
<td>10</td>
<td>1</td>
<td></td>
</tr>
<tr>
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<td></td>
</tr>
<tr>
<td>11</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

What are the next state equations for the circuit?