1. (10 points) What output value is produced by the circuit defined by the VHDL specification shown below, when the input value is 1100?

What unsigned numerical values do the input and output represent?

What common arithmetic function does this circuit implement?

Draw a schematic diagram that is equivalent to the VHDL specification.

```vhdl
library IEEE;
use IEEE.std_logic_1164.all;
entity foo is
  port (A: in std_logic(3 downto 0);
      X: out std_logic(3 downto 0)
    );
end foo;
architecture bar of foo is
begin
  X(0) <= not A(0);
  X(1) <= A(1) when A(0)='1' else (not A(1));
  X(2) <= A(2) when (A(0)='1' or A(1)='1') else (not A(2));
  X(3) <= A(3) when (A(0)='1' or A(1)='1' or A(2)='1') else (not A(3));
end bar;
```