1. (10 points) Is the sequential circuit defined by the VHDL code shown below a Mealy model circuit or a Moore model circuit (circle one or the other)? Draw a state diagram for the sequential circuit. Use the symbolic state names in your state diagram. Be sure to show the outputs and the “self-loops” in the state diagram.

```vhdl
entity foo is
    port (
        clk: in STD_LOGIC;
        A: in STD_LOGIC_VECTOR(1 downto 0);
        X, Y: out STD_LOGIC
    );
end foo;

architecture bar of foo is
    type state_type is (red, green, blue);
    signal state: state_type;
begin
    process(clk) begin
        if clk'event and clk = '1' then
            if state = red and A = "01" then
                state <= green;
            elsif state = red and A = "10" then
                state <= blue;
            elsif state = green and A(1) = '1' then
                state <= blue;
            elsif state = blue and A(1) = A(0) then
                state <= red;
            end if;
        end if;
    end process;
    X <= A(1) when state = red else A(0);
    Y <= '1' when (state = red or state = green) else '0';
end bar;
```