1. In this problem, you are to complete the VHDL module below, so that it implements a sequential circuit with two states, up and down. If the circuit is in the up state, a ‘1’ on the drop input causes it to go to the down state. If it is in the down state and the level output is zero, it goes back to the up state. When it is in the up state, a ‘1’ on the lift input causes the level output to increase by 1, unless it’s already equal to “1111”. When it’s in the down state, the level output decreases by 1 on every clock tick. Your VHDL should be complete and syntactically correct. On reset, the circuit should go to the up state, with level=0.

```vhdl
entity jack is
    Port ( clk, reset, lift, drop: in std_logic;
    level: out std_logic_vector(3 downto 0));
end jack;
architecture Behavioral of jack is
    type state_type is (up, down);
    signal state: state_type;
    signal ilevel: std_logic_vector(3 downto 0);
    begin
        process (clk) begin
            end process;
end Behavioral;
```