1. (10 points) The VHDL module defined below implements a parentheses checker, which determines if the parentheses in an incoming string of ASCII characters are balanced. Complete the block diagram/schematic on the following page so that it corresponds to the circuit specified by the VHDL module. Do this by adding wires and simple gates only.

```vhdl
entity paren is
  Port (
    clk, reset: in std_logic;
    nxtChar : in std_logic_vector(7 downto 0);
    tooDeep, unBal : out std_logic);
end paren;

architecture a1 of paren is
begin
  signal count: std_logic_vector(3 downto 0);

  process (clk) begin
    if clk'event and clk = '1' then
      if reset = '1' then
        count <= "0000";
      else
        if count /= "1111" and nxtChar = x"28" then
          count <= count + '1'; -- x"28" is left paren
        end if;
        if count /= "0000" and nxtChar = x"29" then
          count <= count - '1'; -- x"29" is right paren
        end if;
      end if;
    end if;
  end process;
  tooDeep <= '1' when count = "1111" and nxtChar = x"28" else '0';
  unBal <= '1' when count = "0000" and nxtChar = x"29" else '0';
end a1;
```
What is the smallest clock period for which the circuit is guaranteed to have no internal setup time violations. Assume that all gates have a 1 ns delay, that flip flops have a setup time of 2 ns and a propagation delay of 3 ns and that there is zero clock skew. Also assume that the equality comparison circuits are implemented using exnor gates with outputs anded together and that the increment and decrement circuits are implemented using ripple-carry.