1. (4 points) Draw a logic diagram for a circuit that implements an eight input NAND function using a total of seven simple gates, where each simple gate is either a NAND or a NOR (no inverters). Note that the NAND function is not associative.
2. (6 points) Fill in the Karnaugh map below so that it corresponds to the function
\[ F(A,B,C,D) = \Sigma m(1,4,6,8,11,13), \quad d(A,B,C,D) = \Sigma m(3,5,7,9,12). \]
Derive a minimal sum-of-products expression for this function, taking full advantage of the don’t care conditions.

\[
\begin{array}{cccc}
\text{CD} & \text{00} & \text{01} & \text{11} & \text{10} \\
\text{AB} & \text{00} & \text{01} & \text{11} & \text{10} \\
\text{00} & & & & \\
\text{01} & & & & \\
\text{11} & & & & \\
\text{10} & & & & \\
\end{array}
\]

Draw a logic diagram for a circuit that directly implements your expression using simple AND gates, OR gates and inverters. What is the worst-case delay of the circuit, assuming that every gate and every inverter has a delay of 1 ns?