1. (5 points) Is the sequential circuit shown below, subject to internal hold time violations? If so, show how would you correct them. Assume that the flip flop setup time is 2 ns, the hold time is 1 ns and the flip flop propagation delay ranges from .7 to 2.5 ns. Also, assume that the gate delay ranges from .5 to 2 ns and that the maximum clock skew is 1 ns.

What is the smallest possible clock period for which the circuit will not be subject to internal setup time violations? Take into account the effect of any modifications you made in the first part.
2. (5 points) Draw a state transition diagram for the VHDL module shown below. Don’t forget to show the self-loops.

```
entity foo is port (
    A, clk, reset: in STD_LOGIC;
    X, Y: out STD_LOGIC
);
end foo;

architecture bar of foo is
    type state_type is (red, blue, green);
    signal state: state_type;
begin
    process(clk) begin
        if clk'event and clk = '1' then
            if reset = '1' then
                state <= red;
            else
                if state = red and A = '0' then
                    state <= green;
                elsif state = red and A = '1' then
                    state <= blue;
                elsif state = green and A = '0' then
                    state <= blue;
                elsif state = blue and A = '1' then
                    state <= red;
                end if;
            end if;
        end if;
    end process;
    X <= '1' when state = red else '0';
    y <= '0' when state = green else '1';
end bar;
```