1. (5 points) Is the sequential circuit shown below, subject to internal hold time violations? If so, show how would you correct them (be specific). Assume that the flip flop setup time is 1.5 ns, the hold time is .5 ns and the flip flop propagation delay ranges from .8 to 2.5 ns. Also, assume that the gate delay ranges from .25 to 1 ns and that the maximum clock skew is 1 ns.

What is smallest clock period for which this circuit has no internal setup time violations?
2. (5 points) The diagram at bottom shows a memory array containing 16 words of 2 bits each. Show how the values stored in the memory change as a result of the operations indicated by the timing diagram below.