1. (5 points) For the circuit shown below, assume that the flip flop setup time is 1.5 ns, the hold time is 0.5 ns and the flip flop propagation delay is between 1 and 3 ns. Also, assume that the gate delay is between 0.5 and 2 ns (for all gates) and that the clock skew is 1 ns. What is the smallest clock period for which the circuit is not subject to setup time violations?

During what time period, relative to the clock, must input $A$ be stable.
2. (5 points) Complete the VHDL module shown below, so that it implements the state machine shown at right.

library IEEE;
use IEEE.std_logic_1164.all;

entity foo is
  port (
    clk: in STD_LOGIC;
    A, B: in STD_LOGIC;
    X: out STD_LOGIC
  );
end foo;

architecture bar of foo is

  type state_type is ( );

  signal state: state_type;
  begin
    process(clk) begin
      end process;

end bar;