1. (5 points) Draw a circuit that implements the VHDL code fragment shown below. Use only gates and multiplexors. Assume that $a$, $b$ and $c$ are single bit signals.

```vhdl
x <= "010";
if a = b then x <= z; z <= y;
elsif a > c  z <= "111";
else          z <= a & b & c;
end if;
```
2. (5 points) At what times can the output of a D flip flop change?

At what times can the output a D latch change?

What situation causes a flip flop to become metastable?