1. (5 points) Consider the following VHDL code fragment.

```vhdl
signal x: unsigned(15 downto 0);
signal y: std_logic_vector(10 downto 4);
signal z: unsigned(x'length downto y'left);
...
x(y'right downto z'low) <= (y'right=>’1’, z’low=>’1’, others=>’0’);
z <= y(y’length-2 downto y’low) & y(y’high downto y’length-1);
```

What is the value of \( z’\text{range} \)?

16 downto 10

What is the value of \( x \) in hex?

*intended answer was* \( x = (4 => ‘1’, 10=>’1’, \text{others=>’0’}) = 0000 0100 0001 0000” = x”0410”*

*but in problem statement, the assignment to \( x \) has an empty index range, so this circuit would not synthesize; so this part of the problem was not graded*

If \( y=”1011011” \), what is the value of \( z(13 \text{ downto } 10) \)?

\( z(16 \text{ downto } 10) = y(5 \text{ downto } 4) \& y(10 \text{ downto } 6) = 1110110, \text{ so } z(13 \text{ downto } 10) = “0110” = x”6” \)
2. (5 points) The figure below shows a portion of a simulation of the binary input module with four blanks. Fill in the blanks with the correct values.

List all the possible values of the delta signal.

0001, 0010, 0100, 1000