My Work on All Things Metastable
OR:
(Me and My Glitch)
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It has now been almost 50 years since my first meeting with the glitch. It WAS a meeting. For me, it didn't have the power or majesty of a "discovery". It was more like a meeting. The realization that I had stumbled into a discovery came later. ("Glitch", as I use it here, is slang for the metastable state in a FF (Flip-Flop), or other logic circuit, that has positive feedback with a gain greater than one.) Books written by others (1) (2) encouraged me to record my version of those earlier years. I think keeping history at least somewhat accurate is worthwhile. There is "noise" in recorded history. Each recording of history is from the perspective of the author, and authors are not perfect. The best each of us can do is record what we remember in the hope this will reduce the "noise". Also, for me, there has been a resurgence of metastable activity. Computers are now fast enough that, in a short time period, several FF input timing conditions can be simulated with Spice models. Multiple simulations, using bisection methods to guide the simulations, allow us to analyze a FF's metastable performance in enough detail that the simulations now match the physical test data very well. (3) A new company, Blendics, Inc., is building a packaged tool that exploits the bisection method. This tool will allow designers the ability to analyze their circuits for possible metastable performance without becoming an "expert" in all the ways metastable. Measuring or simulating synchronizers for metastable performance is tricky business. The stimulus signals are quite small and it is easy to get off the track. Simulators have numerical accuracy problems, and real circuit measurements have circuit noise problems. Just identifying the part of the synchronizer circuit that is going metastable can be difficult. The Blendics tool, *MetaACE*, is designed to lead the user through this thicket.

The notion that between any two fixed points of attraction, there is a locus of points where the attraction to the two fixed points is equal has been understood for centuries and was often known as the paradox of Buridan's Ass. The classic question is "Can an ass, when placed exactly between two piles of hay, starve to death?" This is the same issue as the question "can a digital circuit FF remain metastable forever?"

By the time my story starts, metastability in digital FFs had already been discovered several times. There is a saying; "if you are having an idea that is worthwhile, at least ten other people are also having the same idea".[1] Looking back, I can see fragments of some of these other discoveries. There is a paper by S. Lubkin from 1952 (4), and a book by Harry J. Gray (5) published in 1963, but with an over-leaf that states that most of the book is from class notes used since 1958. Lubkin was in New York City

[1] One of Fred Rosenberger's favorite sayings

at the Electric Computer Corporation, and was involved with the ENIAC. Gray helped develop the LACR for Remington Rand Univac, and was a consultant to several other computer companies. (Curtiss Wright Electronics Corp, I T & T, and Philco Corp). Lubkin and Gray were both in the East. It's possible they knew each other.

In 1951, David John Wheeler received the very first PhD in computer science from Cambridge. At Cambridge, he worked on the EDSAC computer and is credited with introducing the "jump to subroutine" command (often called the "Wheeler Jump" command) into computer programming. For two years (1952 and 1953) after receiving his PhD, Wheeler was at the Univ. of Illinois working on the ORDVAC and the ILLIAC. He then returned to Cambridge. Wheeler was also a consultant for Bell Labs and Digital Equipment Corporation Western Research Lab. (6) It's possible that Wheeler knew Gray and/or Lubkin. The first recorded mention of the Glitch by Wheeler I have is from a 1971 talk at the University of Newcastle upon the Tyne, England. (7) In this talk, Wheeler presented a history of the Glitch, including some of the problems it has caused, and a plea to include the Glitch problem in CS and EE classes. There was also work in England at the University of Newcastle that can be traced back to the early 1960s, and there is still active work going on there today. So between 1950 and 1958, (Maybe even in the mid / late 1940s[2]) the Glitch had been noticed by several people who probably traveled in similar circles, attending at least the same conferences.

I knew nothing of this early work for years after my personal story began. I learned about Gray's work just in time to invite him to the 1972 Washington University Workshop, but neither Lubkin's or Wheeler's work was known by us at the time of the 1972 Workshop. I did not learn the location of Lubkin's paper until 1986. (And the reference to the Lubkin paper was given to me by Wheeler!)

My personal story begins in Sept. 1965, when I joined the Computer Systems Lab. at Washington University in St. Louis (CSL) to work on the Macromodule project (8).

While I had been a student in a class at Washington University taught by Jerry Cox and Wes Clark for the semester before joining CSL, this class had nothing to do with the Glitch, or the Macromodule project. Although we did learn about computer hardware design, then designed, built, debugged, and produced a working computer

[2] The ENIAC was funded in 1943 and took 2.5 years to get operational. So the ENIAC was developed during the Second World War, but finished after the end of the war. Both Lubkin and Wheeler write that it was "well known" that incoming asynchronous signals needed to be feed through a pair of clocked FFs. Per both their papers, it was recognized "early on" that the first FF might produce a partial pulse, so a second FF was needed to assure a "full" clock pulse and that one must ONLY use the output from this second FF to avoid logic hazards. Both Lubkin and Wheeler point out that "This solution is logically correct but, in practice, it will not always work" (from Wheeler. (7)) They each go on to discuss how the second FF suffers from metastability problems. Lubkin even discusses using "weighted" outputs to avoid the metastable voltage region, which was the solution I saw when I first looked at the FF waveforms. The pieces were all there to be re-discovered ten to fifteen years later when computing systems were better understood, and a lot less expensive!

in that class. With Severo Ornstein's help, I then wrote a program for that computer that read the keyboard and displayed the keyboard character on a 'scope screen.

When I formally joined CSL, there were already daily meetings attended by Severo , Mish Stucki, and Bob Ellis, to develop some of the high level structure for the macromodule project. I joined this group. Wes Clark would join us from time to time. Mish and Severo shared an office and we met in their office. We worked at a blackboard, and took Polaroid pictures of the board each time it was filled, before ANYTHING was erased. These pictures were taped into a note book. I have a few pictures of this blackboard. Sometimes, I would take an extra photograph of the black board if it was something that I needed to think about or work on. This is the period Severo describes in his book of us trying to find some direction and some idea for a design.(1) We both remember at one of those meetings with Wes where Severo and Mish explained where we were, and then Wes, as he left the room puffing on his pipe, congratulated us on having just re-discovered an existing computer: the ILLIAC III. These meetings would last a couple of hours each day. We would then each go off and work on the issues raised. I spent much of my time learning about ECL circuits, and thinking about how to power this whole thing.

During the fall/winter of 1965, we were working on general schemes. We would design some of the key logic at the level shown in Figure 1, and we would find cases where runt pulses could occur. [3] In some cases, we could work the design down to the point where there was just a single place in the logic where one FF would have to work with an input pulse of any width. One day Severo asked "what happens if this pulse gets small?" I didn't know, so I went off to my office (my "lab" was in my office, it consisted of the WHOLE table next to my desk!) and set up a circuit to try it. I built up a little circuit that had a variable width clock pulse input from a bench pulse generator, and a reset circuit so the FF under test was reset a short time after each runt clock pulse. I used r-c circuits to get the timing about right. Then, for the final tuning, I had a loop of wire about two inches long, looped up off the board by about an inch. I could just bend the wire up and down toward and away from the PC board to get the FF to settle one way or the other. I looked at the resulting display on a 'scope, Figure 2, and said to myself, "all I have to do is avoid the middle region of the voltage swing, and with ECL logic circuits I know how to do that. So there's no problem." I then went back to worrying about "real" issues that I didn't have a CLUE how we were going to solve. From Severo's question to my seeing there was no problem took a week or so. I think I reported at one of the daily meetings that signals arriving at the same time was not an issue, but I didn't even try to explain why.

[3] From Mish Stucki 2012: (In the interest of keeping the recorded history "noise" down.) The circuit shown in Figure 1 is NOT part of the Interlock module that deals with interfacing events from outside the Macromodular system, but is part of a Rendezvous that, when the design was finished, had no Glitch issues. The reason the runt pulse existing when Severo ask the question was because the first general scheme was flawed. When this was recognized and the general scheme was revised, the runt pulse when away for all Macromodular system signaling, except for external inputs. So I had the solution for how to design the Interlock module before the Interlock module was even defined!

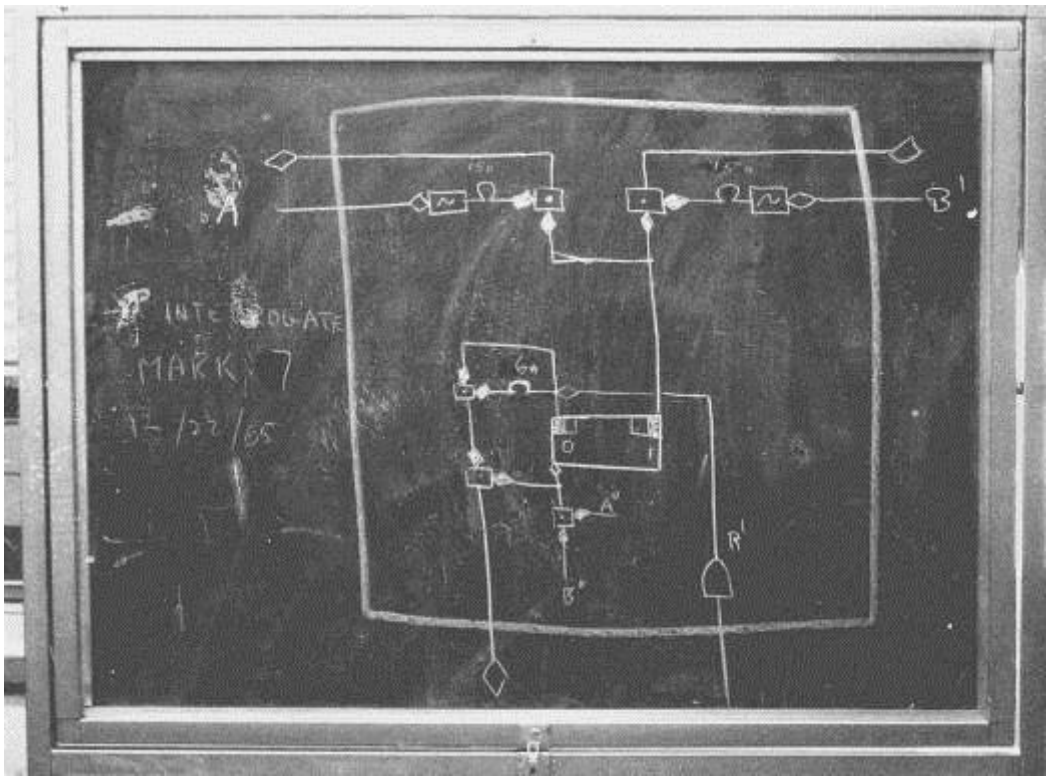


Figure 1

Interrogate circuit design, dated Dec. 22, 1965. This is the "MARK 7" version of the "Interrogate" circuit. This drawing may be the very one Severo pointed at when he asked the question. I took an extra photograph of THIS particular blackboard for some reason. (See footnote 3 above.)

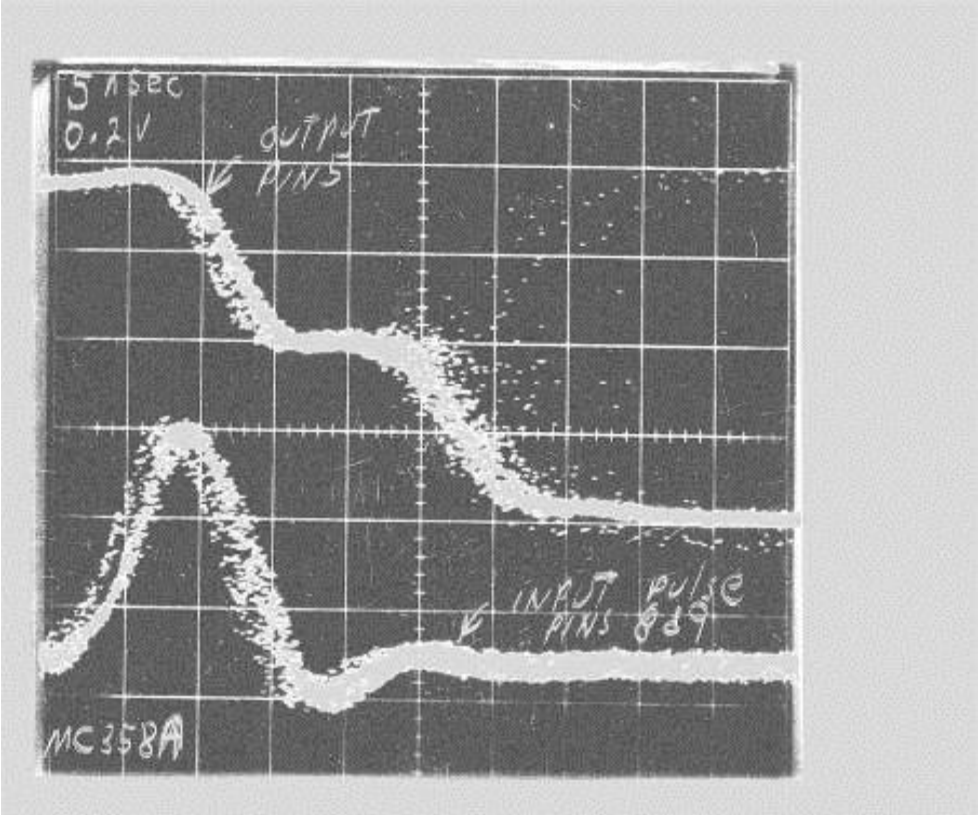


Figure 2.
Early sampling 'scope photo of an ECL-1 FF going metastable (the top trace labeled "OUTPUT PIN 5") in response to a runt clock pulse (Bottom trace labeled "INPUT PULSE PINS 8&9). The package type, the Motorola MC358A, was from the early circuits in TO-5 cans, this all before the DIP package was introduced in 1966.

> No one was sure what happened when the Clock input to a FF received a runt pulse, so I went off and designed a test circuit. I got these results. (There ARE some dots in the output trace going back up toward the positive power supply rail.) I saw the nice defined regions at ¼ and ¾ the signal swing and knew how to design an offset buffer that would have a threshold at ¼ or ¾ the signal swing, and said "there's no problem here.

A few months after I joined, Mackie Littlefield joined the group, and within a few weeks or months after that, Mackie came charging into my office one day excited because Severo had asked him what happened if two signals arrived at a FF at the same time. He didn't have an answer. I still had my little setup, so I showed him. Not a big thing. I didn't have to work very hard to find metastability, so, to me, it was not a big thing, and I was having a little trouble understanding why folks were getting so worked up about all this. Little did I know. . . .

My first “shielded room” was a table top sized copper screen cage made so that the ‘scope and the pulse generator could be put inside the cage with the test FF. This set up allowed me to adjust the test circuit so that longer metastable events were captured. I would get the clock and data timing about right, then use an adjustable delay line to “fine tune” the setup. This was much more stable and allowed me to see longer and longer metastable periods on a ‘scope. While this copper screen cage helped, it became clear that I needed to be in the cage also so I could control the experiment. So the lab acquired a real 8 foot by 12 foot by 8 foot high shielded room in 1967 – 1968.

Early on, I didn't really understand why the waveforms looked the way they did, and was worried about the margins if the bias point of the receiver was offset. It wasn't until, in the hall one day, Russ Pfeiffer told me his model of the Glitch started with a little signal running around two inverters hooked back to back, that was amplified each trip around the loop until the little signal reached full voltage. This was when the light bulb in my head finally turned on. Until then it was all this abstract stuff of balls on hills, pencils on their point, etc. I really didn't have an electronic model of an electronic Flip-Flop in the metastable region in my head. Now, in my mind’s eye, I could see that little electric charge, running around the FF loop, growing as it went. The smaller the charge, the longer it took to grow large enough to be called a “logic level”: a “one” or a “zero”. I could see more than one little charge starting off around the loop. Thinking through starting with multiple little charges let me “see” the common mode effects as well as the difference mode effects. It's amazing how little I knew at the time. I was lucky to be using ECL. If I had done that first experiment with TTL, I probably would have never seen a glitch, and if I DID somehow see metastability, it would have probably been an oscillation type metastability, not a flat middle level, and I would not have seen the easy solution of just detecting the output at a voltage away from the metastable region.

Our primary job in those days was defining and designing the Macromodules. The group split into two smaller groups: One group built up the “phase ½” modules that worked logically, but didn’t have a good power system, cooling system, etc. that were all part of the Macromodule project specification. The other group worked on “the details”. I developed a line of DC/DC converters (my master’s thesis – finished 1969) and worked on the rest of the power system. There was also a lot of work done on air flow and cooling, and just the overall physical structure for the modules was a challenge. Much of the Macromodule design work was finished by 1967 - 1968, I was not involved much in the intense period of work building up an inventory of Macromodules that followed. I designed a couple of “special” DC/DC converters, but for the most part, I returned to collecting glitch data on a number of FFs both ECL and TTL.

In 1973 Wes left and Charlie Molnar became the director of CSL. Charlie was probably THE person that that moved the metastability work from a few papers, as has happened in the 1950s, into a movement that took root and grew into a much

broader understanding of the Glitch. A lot happened in the six years between about 1968 and 1973.

Early on, I took lots of photographs of various kinds of FF going metastable. I was mainly taking real time, analog 'scope photographs that displayed a single event. Many people were hesitant to believe sampling 'scope photographs because they did not fully understand how a sampling 'scope worked. While the sampling 'scope was a great tool to estimate τ (10), it was a poor tool to convince the engineering community that metastability timing was real and could go on for a long time. It seemed that many people would not believe this problem was real. Our goal was to produce enough experimental evidence with photos so that people would at least entertain the idea that the glitch might be a fundamental effect that could not be "solved" with a particular circuit. It seemed that it was necessary to first "get their attention" before they were willing to hear the theory.

As people began to understand the issue, they, of course, wanted some data so they could estimate a MTBF for their systems. My early tests gave a reasonable estimate of τ, but not a very good estimate of T_0. Even so, some of my early plots of data were distributed by Charlie Molnar. We began giving talks at conferences and workshops. Our goal was to convince designers that metastablity was real and could not be designed around. There were theoretical studies that backed up this interpretation of my tests. (9) (10) I made a custom glitch PC board in April of 1972 that contained a bank of counters and some test FF conditioning logic so the test FF could be set to a known state and allowed to "rest" in a known state for a while before the next trial was started. The timing between counters was controlled by ECL buffer packages. The signal delay between counters was carefully measured. The number of metastable state cases remaining vs. time after a trial was started was an exponential decaying function.

The use of circuit simulators, such as Spice, were becoming useful as a general tool, but the transistor models available to us were not good enough for us to match simulation and experimental results except to see that the trend of the circuit operation was the same. Also, the simulations would fail to converge. In order to make real use of simulators, we needed (a) better transistor models, (b) bigger, faster computers, and (c) to understand that the bisection techniques could help us avoid the simulation convergence issues. Some of these are just now becoming available to us.

In reviewing lots of designs and looking for the node, or nodes, in the circuit that went metastable, we found designs where, when trying to avoid metastability, the designer had introduced a logic hazard that would make the reliability hundreds of times worse than it needed to be. Designers resorted to other kinds of logic. Some claimed that tunnel diode circuits would not have metastable problems, others saw the Schmitt Trigger circuit as the savior. Of course, none of the schemes were free of the Glitch.

In about 1967, Mackie and I went off to an electronics show in Chicago where Motorola had a booth. A new line of ECL was being introduced, the MECL-III line I think. Mackie asked the guy at the booth what happens to one of these new super fast flip-flops if the data to clock timing was "just so". To our surprise, the guy answered! The guy turned the booth duties over to someone else, and we went off to talk. That "guy" was Ivor Catt, who had published a paper in the IEEE transactions in 1966. (11) Ivor told us that he had so much trouble getting the reviewers to accept the paper, that in the end, it was hard to read and he had received NO responses from any reader of his paper. This was the first we had heard about Ivor's paper.

In the meantime, we seemed to be making some headway in getting others to understand the Glitch. With my photographs of all manner of FF going metastable and the other work on the theory, Charlie's showing of the photographs at the Dec. 1971 ARPA IPT contractors' meeting, and at a modular computer systems workshop in St. Louis at about the same time, we generated some interest in a workshop on the Glitch. This workshop brought the fragments of metastability work from around the world together. By this time, six years after we had found the problem, I had collected lots of data, and people from other universities and companies had some data also. The results of my experimental work had been distributed to some interested parties. Washington University had produced several internal technical notes and a doctorate dissertation. (10) Also, we were seeing some interest in the Glitch because products were failing. So in April of 1972, we held a workshop at a retreat center Washington University owned. There were about 30 people at this conference. It was quite a mix of people; some from other universities, some from France, some from England, some from industry. Some were invited, and some had asked us if they could attend because they had a problem to solve. There were about 10 from WU. Chuck Seitz (Chapter 7 of Mead and Conway)(12) was there, David Gray (who put metastability in his textbook so many years before this conference), Ivor Catt, Severo (by now at BB&N working with the team that built the first part of the Arpanet) I think this workshop was very important in giving the Glitch traction. This workshop could be the point where metastability became "real". This workshop spread seeds that reinforced each other so that each attendee could stand up and proclaim metastability is real, and it is a real problem in computing systems. A key part of an invitation to this workshop was that each person had to present his work, or his problem. We had papers on real world failures, theory papers, philosophical talks, and several papers from WU folks. Charlie felt that that this conference should not be recorded. He felt that the tradeoff between getting the attendees to really tell us what was going on was more important than having a recording. The outcome of this workshop was in the heads of the attendees.

In the early 1970s, we tried to publish some papers. I sent a letter to the editor of Electronics Magazine. My note was rejected because Electronics Magazine does not print articles on fundamental principles, but the letter went on to say that if I came up with a solution to the problem, they would be happy to publish that. Some others,

including Bob Couranz, were turned down by various IEEE publications. A couple of years later, the rejected papers were accepted for publication. In the midst of these rejections, Charlie received a call from a Scientific American reporter. The reporter had heard about the workshop on metastability and understood this caused computer failures. He had also talked to Severo and someone at Digital Equipment Corp. Out of this came a short note in the Apr. 1973 issue of Scientific American that mentioned our workshop and included a quote that an experimental Digital Equipment Corporation machine failed once an hour. (13)

By early 1973, I had figured out how to drive many types of FFs metastable and had data and photographs. I had my custom glitch test board, a good collection of high grade coax cable, including a selection of both fixed and adjustable air lines that I used as delay lines. The signal propagation through these air lines was specified to better than ± 0.18%. I could accurately add and subtract sections of air line to adjust the timing of the setup. If I had a total of 10ns of air lines, I could count on the delay being 10ns within 80ps. All this allowed me to have good control of the timing change needed to produce different outputs. I had developed a power supply voltage feedback scheme so that I could allow a test to run for hours, to even a few days and the FF under test would remain near the metastable point with the FF resolving both high and low. I did much of this testing inside the shielded room. One big advantage of the room was no windows. With the door shut, it was quite dark. I even placed black tape over the lights on the equipment to block even that light. I was trying to see, and record on film, a single faint trace across the 'scope screen. By sitting in the dark, the "afterglow" from the 'scope screen would die out after a few minutes. I could then open the camera shutter without fogging the film. The dark room allowed me to view the waveforms until I had a setup I wanted to photograph. I would then mount the Polaroid camera in front of the 'scope screen, open the camera shutter, and enable the 'scope trigger circuit, then wait for a few minutes until a trace came along. My eyes would also adjust so I see the single trace better. Sitting there, watching the 'scope screen, I developed an understanding of how various inputs affected the performance of the various kinds of FFs. I was testing FFs from other logic families in order to record events that remained metastable for long periods of time to show that all families of FFs could be driven metastable. The need to "show and tell" in place of telling the "theory of why" about metastability was still needed to get people's attention. We were still talking about metastability to other research groups, and some companies. We were still spreading the word.

Mackie did most of the writing of our Technical Memo in 'Dec. '66. There were also some other Technical Memo papers written, but no real distribution outside the university. The first published papers on metastability by any of us were in 1972 and '73. In fact, the first writing of a paper was after some prodding from Severo, who threatened to write a paper on his own if we, who he felt SHOULD write the paper, didn't "get on the stick". Severo, Mackie, and I wrote one paper for a conference (14), and Charlie and I wrote another paper for the IEEE Computer Transactions. (15) The Chaney/Molnar paper was carefully written to only include

claims we could prove. The photographs were not enhanced in any way. There are no equations in this paper. There is not even a suggestion of any exponential timing relationships, only that there is some "anomalous behavior" at the output. The paper, two pages long, has a total of 6 photographs, some description of the photographs, and a statement that we have not seen much published on this subject. This paper does note that there was a recent workshop at WU on this subject where it was revealed that computer systems from several manufactures have significant system failure rates.

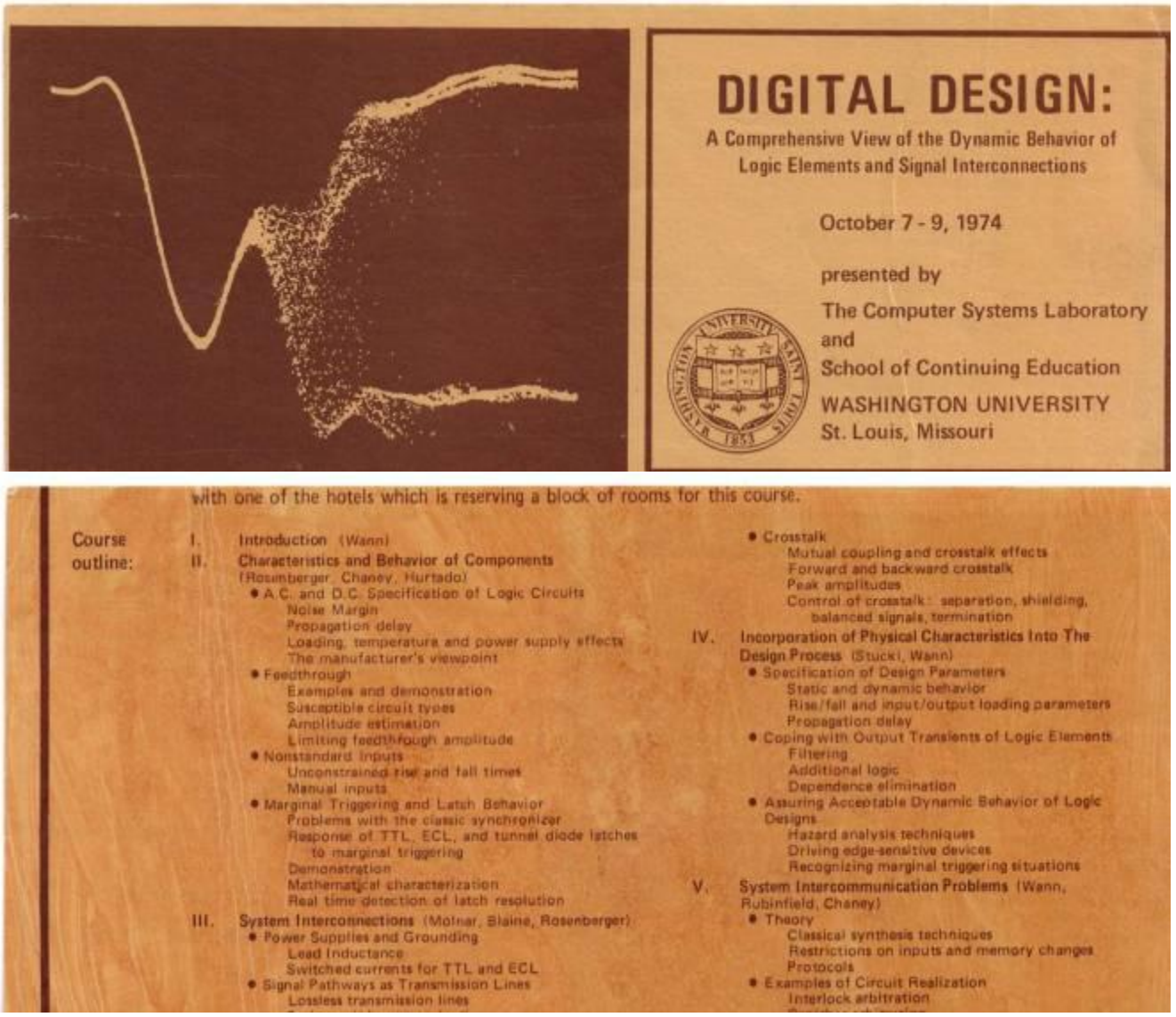
Until 1974, my glitch testing was done with a fixed clock-to-data timing. The general scheme was to adjust the clock–data timing right at the metastable point to get the maximum number of Glitches per second. This method of testing produced data that was hard to use to design synchronizers. One could calculate the probability of a metastable event still going on for any time after the clock, FOR THE DATA SIGNAL TIMING USED to collect the data. In the presence of noise, the range of the data input timing was unknown. From lots of testing, I knew the timing range of the data signal, from the FF always setting to the FF never setting, was on the order of 30ps. At the speed of light in air, light travels 1cm in about 30ps. With the adjustable air lines, I could adjust the air line length to within about ½ mm, so I could set the signal timing to within 1 ps or so. 1 ps is a much smaller value than the width of the signal edge timing jitter. I typically had a ruler taped to the adjustable air line so I could measure, with the ruler, the timing to within 1 ps. Having spent time getting comfortable with the timing capabilities of this setup was important to allow me to see the next step in characterizing metastable FF performance. Also, the adjustable air lines were called "trombones" as the air lines were about the same diameter as the slides on a musical trombone, and the two sections of the air line slid past each other much like a trombone.

Partly because of the success of the Apr. 1972 Workshop on the Glitch, Charlie organized a Digital Design short course for October 7-9, 1974. The cover of the advertising brochure that went out had a sampling 'scope photograph showing metastability. (Figure 3) Several attendees said they came because of the brochure cover. I was working hard on getting good, solid data and photographs for this short course. Part of the issue was how to characterize the effective width of the data signal input noise. One day, a few weeks before the short course, Charlie called Don Wann, me, and maybe some others, into our conference room and stood at the black board and worked out the equations under the assumption that the clock and data signals were uniformly distributed over a whole clock period. While watching this development, I realized that if (a) I let the FF under test rest for a while between trials so there was no history dependence between trials, then (b) A uniform sweep of the input timing was just as good as an equal number of random inputs. And (c), I could get a uniformly changing delay if I put a motor driven screw drive on one of the adjustable air lines. Charlie recounted later that, at this point, I ran from the room shouting "motorized trombone!" I took one of the adjustable air lines and to the machine shop, where I had a motor drive made for the air line. The machinist,

George Meyer, did his standard excellent job of creating what I needed.[4] The motor drive would advance or retard the air line at about an inch per minute, so lots of samples of metastability were collected during one sweep of the air line, ten million to one hundred billion samples. I re-did all my tests before the Oct. 1974 workshop. This scheme of data collection is explained in my three page 1983 paper (16) that presents a page sized table of data from many different types of FF along with two pages of notes on the table, and in a paper Fred Rosenberger and I wrote at about the same time.(24) The key observation is that "data timing uniformly distributed over a clock period" includes all data–clock timing relationships that produce unstable results. However, it's only those data-clock timing relationships that usually fit within a small window, someplace between the setup and hold times for the FF, that need to be tested. The motorized delay line could be adjusted over a full ns of time. So, with a single sweep of the input timing, I covered all the interesting cases. The data inputs over the rest of the clock period would all be within the setup and hold limits and thus the FF would produce no metastable events. So the data we collect of metastable events over our sweep of the clock data timing is the same as the data we WOULD collect if we sweep over a full clock period.

We were also beginning to do circuit simulations using spice. The Spice models we were using were simple transistor models. Fred Rosenberger and Don Wann were more involved with the simulation efforts than I. I remember that, as part of the '74 short course, Don wanted to show some simulation results along with his other analysis of a TTL 7474 FF. We failed in getting a simulation of any metastable operation of the 7474 type FF. The simulation would run up to about the point the internal nodes were nearing metastability, then the simulation would abort with a "step size too small" message. For us at least, the beginning of how to break through this problem had to wait another year.

[4] At CSL, in addition to the technician staff, we had a PC board fabrication facility and a machine shop with a very skilled machinist. The importance of a good staff and the effect that has on productivity is often over looked.



DIGITAL DESIGN:

A Comprehensive View of the Dynamic Behavior of Logic Elements and Signal Interconnections

October 7 - 9, 1974

presented by

The Computer Systems Laboratory
and
School of Continuing Education
WASHINGTON UNIVERSITY
St. Louis, Missouri

with one of the hotels which is reserving a block of rooms for this course.

Course outline:

I. Introduction (Wann)

II. Characteristics and Behavior of Components (Rosenberger, Chaney, Hurtado)
- A.C. and D.C. Specification of Logic Circuits
  - Noise Margin
  - Propagation delay
  - Loading, temperature and power supply effects
  - The manufacturer's viewpoint
- Feedthrough
  - Examples and demonstration
  - Susceptible circuit types
  - Amplitude estimation
  - Limiting feedthrough amplitude
- Nonstandard Inputs
  - Unconstrained rise and fall times
  - Manual inputs
- Marginal Triggering and Latch Behavior
  - Problems with the classic synchronizer
  - Response of TTL, ECL, and tunnel diode latches to marginal triggering
  - Demonstration
  - Mathematical characterization
  - Real time detection of latch resolution

III. System Interconnections (Molnar, Blaine, Rosenberger)
- Power Supplies and Grounding
  - Lead Inductance
  - Switched currents for TTL and ECL
- Signal Pathways as Transmission Lines
  - Lossless transmission lines
- Crosstalk
  - Mutual coupling and crosstalk effects
  - Forward and backward crosstalk
  - Peak amplitudes
  - Control of crosstalk: separation, shielding, balanced signals, termination

IV. Incorporation of Physical Characteristics Into The Design Process (Stucki, Wann)
- Specification of Design Parameters
  - Static and dynamic behavior
  - Rise/fall and input/output loading parameters
  - Propagation delay
- Coping with Output Transients of Logic Elements
  - Filtering
  - Additional logic
  - Dependence elimination
- Assuring Acceptable Dynamic Behavior of Logic Designs
  - Hazard analysis techniques
  - Driving edge-sensitive devices
  - Recognizing marginal triggering situations

V. System Intercommunication Problems (Wann, Rubinfield, Chaney)
- Theory
  - Classical synthesis techniques
  - Restrictions on inputs and memory changes
  - Protocols
- Examples of Circuit Realization
  - Interlock arbitration

(Figure 3)

The brochure used to advertise a short course we gave in 1974

There were others working on formal proofs that metastability exists. In addition to Bob Couranz, Marco Hurtado finished his dissertation with a formal proof that includes the effects of noise. (17) Also, we did get our interlock module for the Macromodules designed and built. Maury Pepper took my offset voltage design and used that element to design the interlock module. Severo was involved in that design. There was also work done by Warren M. Littlefield (Mackie), K. Karada, and Bob Couranz, who all wrote Technical Memos on interlock designs.

The bisection approach, which was a break through that allows simulators to avoid numerical precision problems on long simulation runs, has some seeds at WU in about 1975. Charlie was in Holland for a year. He had Fred and me doing some simulation of a particular FF under a small government contract. Our simulations bogged down, as they often did, before the simulation got to the interesting region. Charlie asked me to plot some of the results with the input timing set near the point at which the simulations bogged down. And low and behold, the data could be fit to a straight line! That first plot I did for him became one of the HP video taped CEM lecture slides. (Figure 4) (18) There are probably other beginnings of this process, but this one I knew about and took a part in. This approach is based on an old idea. If you take any continuous curve and zoom in enough, the section of the curve you have left after the zoom approaches a straight line. For cases, such as metastability analysis, where the voltage at the input nodes demanded better numerical accuracy than at the output nodes, restarting the simulation at a later time allows the simulation to progress again until the new input nodes again demanded numerical accuracy that was not achievable. (Defining “not achievable” takes some thought and work. See MetaACE white papers.) This process can be repeated as needed to simulate longer and longer resolving times, leaving behind a trail of values that relate the input and output of the last simulation run. The product of these values can be related to the original input timing conditions with a single value, Charlie called this single value the "time gain" as it related an input timing between clock and data to a set of voltage values recorded at a later simulated time.

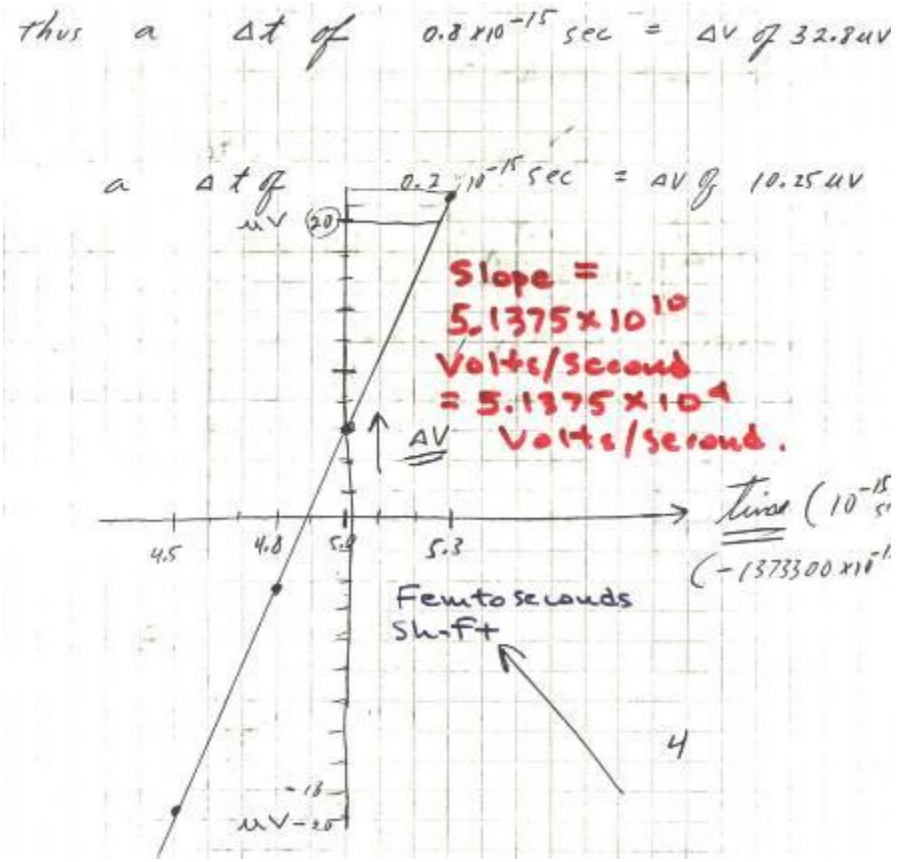


Figure 4

This plot is from my notebook and is in Charlie's slide set for the HP videotaped lecture. This may be the beginning of the bisection method.

We were convinced that metastability was a fundamental problem by 1966 and, over the years, had spent a lot of time and energy convincing others. At the end of my Wormald rebuttal paper, dated Oct. 1979, I wrote: "In closing, there is a great deal of theoretical and experimental evidence that a region of anomalous behavior exists for every device that has two stable states. The maturity of this topic is now such that papers making contrary claims without theoretical or experimental support should not be accepted for publication."(19)

From our first "discovery" (Dec 1964) to the Chaney/Molnar paper (written in 1972) is about 7 years. We are now looking back from 2012, or about 47 years. As viewed from now, 7 years seems like little more than a spot in time. I wrote a

Bibliography of work on Synchronizers and Arbiters that I had kept up to date until about 1990. (20) A better bibliography is now available from Ian Clark. (21). During the 1980s, I did some testing under contract. I wrote up the 15 years of my life into a big table with two pages of footnotes.(16) Fred Rosenberger and I also wrote a paper that explains the details of my test method.(24) By 1990, my primary focus was elsewhere. I even stopped reading about the Glitch, metastability, synchronizers and arbiters[5]. In the background, Jerry Cox continued to work on mixes of synchronous and asynchronous systems with a goal of evolving a procedure that would take a designer from a very high level description of a computing system all the way to an IC layout. This work has reached the point, that in 2007 the company Blendics, Inc. was formed. As one might guess, knowing the parameters associated with metastability are an important input to the design process.

Now that I have re-joined the metastability community, I find there are annual international conferences with many of the conference papers on metastability. The basic bisection scheme, that perhaps started in 1975, has been detailed in papers and a book. (22) (23) A lot has been done, and there are several groups in industry with the primary job of finding the metastability constants for that companies products. It does not appear that a champion has yet immerged that can be looked up to as the "reference". Perhaps *MetaACE* will claim that spot. Blendics has now been working on a tool for years that has an input of a circuit model, and an output of the MTBF of that circuit, with displays of several intermediate points of the process that computes MTBF. We think we are close to having a solid product, but there have been many twists and turns in making sure we have accounted for everything.

Ivan Sutherland, who was the funding officer at DARPA for the Macromodular project, has said that just the glitch work that came out of the Macromodular project more than justified the expense of the whole program. Perhaps the best thing I can say in conclusion is that I did do the tests, and the Glitch became much better known and understood as a result. All this development was not just me. There were about twelve different people at WU who were involved enough to have written papers on different aspects of the Glitch, and there were many more who contributed, but did not write a paper. The study and teaching of metastability has continued through the years at Washington University in St. Louis, and I have been privileged to be a part of that development, including my current involvement in Blendics.

[5] Even though I claim I was no longer involved, the license plate "number" on my car has been "GLITCH" for about 15 years now.

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