
2. Show how the sequential circuit shown below can be mapped onto a single configurable logic block. Do this by specifying the functions that the LUTs implement and showing the paths through the multiplexors that must be configured to provide the required connections (show this by drawing heavy lines on a photocopy of page 6-21 of the notes). Also show what values must be stored in each location of the LUTs to implement the required logic functions.

3. Extend the simple processor covered in section 7 of the notes to include a subtraction instruction. The instruction should be identified by an operation code of 1010 in the first four bits. The remaining 12 bits should include the address of a memory word. The value in this word is to be subtracted from the contents of the accumulator and the result saved in the accumulator.

Create a timing diagram similar to those on page 7-25 of the notes. Use this to guide you in the design process for your instruction.

You will find the VHDL source for the processor on the web site. Modify this to implement the subtraction instruction and verify that it works correctly by simulating the operation of the subtraction instruction (that is, initialize the RAM with a short program that uses the subtraction instruction and simulate the operation of the processor as it runs this program). Turn in copies of those VHDL modules you had to change and mark all the lines that were modified or added.

Note, the processor takes about 30 minutes to synthesize (results will vary depending
on speed of your computer). Also, the synthesizer produces a number of warnings that you may ignore. When you simulate the circuit, you may get a message from the simulator complaining that multiple buffers are attempting to drive the same wire. You may ignore this as well.