1. Enter schematics for the SR master-slave flip flop and for the D edge-triggered flip flop in the schematic editor, using just NAND gates and inverters. Simulate the flip flops with the input waveforms shown below. Use the unit delay mode with a clock period of 40 ns and with the simulation precision set to 1 ns.

2. MK 4-13.

3. Analyze the sequential circuit shown below. Write the output equations and the next state equations. Also show both the state transition diagram and the state table. Is this a Mealy machine or a Moore machine?

4. MK 4-11.

5. Design a sequential circuit that determines if the number of 1s in an input data stream is divisible by 3 or not. Your circuit will have a data input \( D \), an enable input \( EN \) and a clock input. It will also have a single output \( Z \). When \( EN = 0 \), \( Z = 1 \). After \( EN \) goes
high, your circuit will observe the number of 1s in the incoming data stream and whenever the number of 1s seen so far is divisible by 3, the output Z, will be 1. At all other times it will be zero. The serial parity generator on page 4-9 of the notes performs a similar function.

Create a state transition diagram for your circuit (it should have 3 states). Write down the output equation and the next state equations. Create a schematic that implements your design and enter it using the schematic editor. Finally, simulate your circuit, using the unit delay mode, with a simulator precision of 1 ns and a clock period of 20 ns.