CS/EE 260 - Homework 9

Due 4/16/2001

1. (20 points) Consider the program on page 1-21 and 1-22 of the lecture notes. Suppose the simple processor is augmented with a direct-mapped instruction cache with 16 words. Each cache word includes a tag, consisting of the upper 12 bits of the stored instruction’s address and the instruction itself. Assume that all words in the cache are zero at the time the program starts execution. Show the contents of the cache the first time that the instruction at location 000a is executed. Show the contents of the cache the second time that the instruction at location 000a is executed. Show the contents of the cache the third time that the instruction at location 000a is executed.

Suppose that an instruction fetch takes 2 clock cycles for instructions that are present in the cache, but 10 clock cycles for instructions that are not in the cache. How much time is spent on instruction fetches during the first execution of the loop in the program on 1-21 and 1-22? How much time is spent on instruction fetches during the second execution of the loop? Explain your answers.

2. (30 points) This problem involves extending the simple processor presented in class. In particular, you are to add a new conditional branch instruction that branches to a specified location when the value in the accumulator is greater than or equal to zero. Use B as the operation code for your new instruction. So, an instruction of the form Bxxx will cause the program counter value to change to xxx if the ACC is greater than or equal to zero, otherwise it will increment to the next instruction, as it normally does.

Turn in a copy of the VHDL code, highlighting all lines that you changed, and including a brief comment explaining what each added or modified code segment does. Simulate your design, by pre-loading the memory with a small test program that exercises the new instruction, showing both when it branches and when it does not branch. Turn in simulation output that shows the values of all the processor registers and the two buses, during the execution of your test program. On the simulation output, highlight the places where your new instruction is used.