1. For each of the sequential circuits shown below, write the next state and output equations, then create a state transition table and a state transition diagram for the circuit. Be sure to use the correct format for your transition diagrams (Mealy vs. Moore).
2. For each of the state transition diagrams show below, create a transition table, then derive the next state and output equations. Show the Karnaugh maps used in the derivation of the next-state and output equations. Finally, draw a sequential circuit that implements the state diagram.
3. For each of the circuits in Problem 1, draw a timing diagram like the one on page 4-8 of the lecture notes showing the time periods during which the inputs must be stable. For each of the Moore model circuits, also show the time periods during which the outputs may be changing. Assume that the flip flop setup time is 2 ns, the hold time is 1 ns, that gate delays for simple gates can range from .4 ns to 1.5 ns, that gates with 3 or 4 inputs have the same delay as two simple gates and that the flip flop propagation delay can range from 1 ns to 4 ns.

4. For each of the circuits in Problem 1, determine if the circuit is subject to internal hold time violations. If so, show how to modify the circuit to eliminate the hold time violations. If not, explain why not. Assume that the flip flop setup time is 2 ns, the hold time is 1 ns, that gate delays for simple gates can range from .3 ns to 1.5 ns, that gates with 3 or 4 inputs have twice as much delay as simple gates, that the flip flop propagation delay can range from 1 ns to 4 ns and that the clock skew is 1 ns.

5. For each of the circuits in Problem 1, determine the shortest clock period that can be used without causing any internal setup time violations. What maximum clock frequency does this correspond to? Assume that the flip flop setup time is 2 ns, the hold time is 1 ns, that gate delays for simple gates can range from .4 ns to 1.5 ns, that gates with 3 or 4 inputs have twice as much delay as simple gates, that the flip flop propagation delay can range from 1 ns to 4 ns and that the clock skew is 1 ns.