1. For each of the sequential circuits shown below, write the next state and output equations, then create a state transition table and a state transition diagram for the circuit. Be sure to use the correct format for your transition diagrams (Mealy vs. Moore).

Output equations: \( X = S_0 B + A \overline{B} \quad Y = A + S_0 \overline{B} \)

Next state equation: \( D_0 = A \overline{B} + S_0 A \overline{B} \)

<table>
<thead>
<tr>
<th>( S_0 )</th>
<th>( A )</th>
<th>( B )</th>
<th>( D_0 )</th>
<th>( X )</th>
<th>( Y )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
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<td>0</td>
<td>1</td>
<td>1</td>
<td>11</td>
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<td>01</td>
<td>0</td>
</tr>
</tbody>
</table>
Output equations: $X = S_1 + S_0'$  $Y = S_0$

Next state equation: $D_1 = S_1A'B' + S_1S_0B + S_0A'B$  $D_0 = A'B' + S_0A' + S_1B' + S_1S_0$

<table>
<thead>
<tr>
<th>$S_1S_0$ $AB$</th>
<th>$D_1D_0$ $XY$</th>
</tr>
</thead>
<tbody>
<tr>
<td>00 00</td>
<td>01 10</td>
</tr>
<tr>
<td>00 01</td>
<td>11 10</td>
</tr>
<tr>
<td>00 10</td>
<td>01 10</td>
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<tr>
<td>00 11</td>
<td>00 10</td>
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<td>01 00</td>
<td>01 01</td>
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<td>01 01</td>
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<td>01 10</td>
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<tr>
<td>11 10</td>
<td>00 11</td>
</tr>
<tr>
<td>11 11</td>
<td>00 11</td>
</tr>
</tbody>
</table>
Output equations: $X = S_0' + S_1B'$

Next state equation: $D_1 = AB' + S_1S_0'A + S_1S_0B + S_1S_0B'$  
$D_0 = (S_1 \oplus S_0 \oplus B)A' + (S_0 + B)A$

<table>
<thead>
<tr>
<th>$S_1S_0$</th>
<th>$AB$</th>
<th>$D_1D_0X$</th>
</tr>
</thead>
<tbody>
<tr>
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<td>11 0</td>
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<tr>
<td>11</td>
<td>11</td>
<td>11 0</td>
</tr>
</tbody>
</table>
Output equations: \( X = S_2 + S_1 S_0 \) \( Y = S_1 S_0 \)

Next state equation:
\[
D_2 = S_2 S_1 S_0 A' + S_1 A (S_2' + S_0) \\
D_1 = S_2 S_1 S_0 A' + S_1 S_0 (S_2 + A) \\
D_0 = S_2 S_1 S_0 A' + S_2 (S_0 A + S_1 (S_0' + A))
\]

<table>
<thead>
<tr>
<th>( S_2S_1S_0A )</th>
<th>( D_2D_1D_0XY )</th>
</tr>
</thead>
<tbody>
<tr>
<td>000 0</td>
<td>001 00</td>
</tr>
<tr>
<td>000 1</td>
<td>101 00</td>
</tr>
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<td>001 10</td>
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<tr>
<td>110 1</td>
<td>000 10</td>
</tr>
</tbody>
</table>
2. For each of the state transition diagrams show below, create a transition table, then derive the next state and output equations. Finally, draw a sequential circuit that implements the state diagram.

<table>
<thead>
<tr>
<th>$S_0$</th>
<th>$AB$</th>
<th>$D_0$</th>
<th>$XY$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
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<td>0</td>
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<td>10</td>
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<tr>
<td>1</td>
<td>11</td>
<td>0</td>
<td>01</td>
</tr>
</tbody>
</table>

\[ D_0 = S_0'B + A'B + S_0'AB' \]

\[ X = S_0'B + (A' + S_0)B' \]

\[ Y = S_0'A + S_0(A' + B) \]
\begin{align*}
S_1 S_0 \ AB & \quad D_1 D_0 \ XY \\
\hline
00 & 00 & 10 & 10 \\
00 & 01 & 00 & 10 \\
00 & 10 & 10 & 10 \\
00 & 11 & 11 & 10 \\
10 & 00 & 11 & 00 \\
10 & 01 & 11 & 00 \\
10 & 10 & 10 & 00 \\
10 & 11 & 10 & 00 \\
11 & 00 & 10 & 01 \\
11 & 01 & 11 & 01 \\
11 & 10 & 11 & 01 \\
11 & 11 & 00 & 01 \\
\end{align*}

\begin{align*}
D_1 &= S_1 A' + B' + S_0 A \\
D_0 &= S_1 S_0 A' + S_1 A' B + S_1 A'B + S_0 A B' \\
\end{align*}

\begin{align*}
\begin{array}{c|cccc}
\text{AB} & 00 & 01 & 11 & 10 \\
\hline
S_1 S_0 & 1 & 0 & 1 & 1 \\
x & x & x & x & x \\
1 & 1 & 1 & 0 & 1 \\
x & x & 1 & 1 & 1 \\
\end{array} & \quad \begin{array}{c|cccc}
\text{AB} & 00 & 01 & 11 & 10 \\
\hline
S_1 S_0 & 0 & 0 & 1 & 0 \\
x & x & x & x & x \\
0 & 1 & 0 & 1 \\
1 & 1 & 0 & 0 \\
\end{array} & \quad x = S_1' \\
& \quad y = S_0' 
\end{align*}
\[
S_1S_0AB = D_1D_0X \\
\begin{array}{c|c|c|c|c}
S_1S_0 AB & D_1D_0 X \\
\hline
00 00 & 11 0 \\
00 01 & 01 1 \\
00 10 & 10 0 \\
00 11 & 10 0 \\
01 00 & 01 1 \\
01 01 & 00 1 \\
01 10 & 11 1 \\
01 11 & 11 1 \\
10 00 & 11 0 \\
10 01 & 00 1 \\
10 10 & 11 0 \\
10 11 & 11 0 \\
11 00 & 00 1 \\
11 01 & 10 1 \\
11 10 & 11 0 \\
11 11 & 11 0 \\
\end{array}
\]
\[
D_1 = S_0'B' + S_1'A + S_0A + S_1S_0B \\
D_0 = S_0'AB' + S_1'S_0'A' + S_0A + S_1S_0'B' \\
X = S_0'A' + S_0'S_1 + A'B
\]
3. For each of the circuits in Problem 1, draw a timing diagram like the one on page 4-8 of the lecture notes showing the time periods during which the inputs must be stable. For each of the Moore model circuits, also show the time periods during which the outputs may be changing. Assume that the flip flop setup time is 2 ns, the hold time is 1 ns, that gate delays for simple gates can range from .4 ns to 1.5 ns, that gates with 3 or 4 inputs have the same delay as two simple gates and that the flip flop propagation delay can range from 1 ns to 4 ns.

(a) There are 3 gate delays between a change in A and a change at a flip flop input. So A must be stable starting at \((2 + 3 \times 1.5) = 6.5\) ns before the clock changes and must stay stable until \((-1 + 3 \times .4) = .2\) ns before the clock changes. Input B is also delayed by 3 gate delays, hence has the same timing requirements. The timing diagram appears below.

(b) There can be 4 or 5 gate delays between a change in A and a change at a flip flop input. So A must be stable starting at \((2 + 5 \times 1.5) = 9.5\) ns before the clock changes and must stay stable until \((-1 + 4 \times .4) = .6\) ns before the clock changes. Input B can also be delayed by either 4 or 5 gate delays, hence has the same timing requirements. Output X can be delayed by either 1 or 2 gate delays, which means it can change from \((1 + 1 \times .4) = 1.4\) ns after the clock changes until \((4 + 2 \times 1.5) = 7\) ns after the clock changes. Output Y is delayed by 0 gate delays, which means it can change from 1 ns after the clock changes until 4 ns after the clock changes.
(c) There can be 2 to 4 gate delays between a change in A and a change at a flip flop input. So A must be stable starting at \((2 + 4 \times 1.5) = 8\) ns before the clock changes and must stay stable until \((1 - 2 \times 4) = .2\) ns after the clock changes. Input B can be delayed by either 4 or 5 gate delays, so must be stable starting at \((2 + 5 \times 1.5) = 9.5\) ns before the clock changes and must stay stable until \((-1 + 4 \times 4) = .6\) ns before the clock changes.

\[
\begin{array}{c|c|c|c|c}
0 & -5 & 0 & +5 \\
\hline
CLK & A & B & & \\
\end{array}
\]

\[
\begin{array}{c|c|c|c|c}
-9.5 & -8.1 & +0.2 & & \\
\hline
A & & & & \\
\end{array}
\]

\[
\begin{array}{c|c|c|c|c}
-9.5 & -0.6 & & & \\
\hline
B & & & & \\
\end{array}
\]

(d) There can be 3 to 5 gate delays between a change in A and a change at a flip flop input. So A must be stable starting at \((2 + 5 \times 1.5) = 9.5\) ns before the clock changes and must stay stable until \((-1 + 3 \times 4) = .2\) ns before the clock changes. Output X can be delayed by either 1 or 2 gate delays, which means it can change from \((1 + 1 \times 4) = 1.4\) ns after the clock changes until \((4 + 2 \times 1.5) = 7\) ns after the clock changes. Output Y can also be delayed by 1 or 2 gate delays.

\[
\begin{array}{c|c|c|c|c}
0 & -5 & 0 & +5 \\
\hline
CLK & A & X & Y & \\
\end{array}
\]

\[
\begin{array}{c|c|c|c|c}
-9.5 & -8.1 & +1.4 & +7 \\
\hline
A & & & & \\
\end{array}
\]

\[
\begin{array}{c|c|c|c|c}
-9.5 & -0.6 & +1.4 & +7 \\
\hline
B & & & & \\
\end{array}
\]

\[
\begin{array}{c|c|c|c|c}
+1.4 & +7 & & & \\
\hline
X & & & & \\
\end{array}
\]

\[
\begin{array}{c|c|c|c|c}
+1.4 & +7 & & & \\
\hline
Y & & & & \\
\end{array}
\]
4. For each of the circuits in Problem 1, determine if the circuit is subject to internal hold time violations. If so, show how to modify the circuit to eliminate the hold time violations. If not, explain why not. Assume that the flip flop setup time is 2 ns, the hold time is 1 ns, that gate delays for simple gates can range from .3 ns to 1.5 ns, that gates with 3 or 4 inputs have twice as much delay as simple gates, that the flip flop propagation delay can range from 1 ns to 4 ns and that the clock skew is 1 ns.

(a) In the first sequential circuit there is a path from the flip flop output to the flip flop input with just two gate delays. Since \(1 + 2 \times 0.3 < 1 + 1\), we would normally conclude that this does have an internal hold-time violation. However, since we are going from the output to the input of the same flip flop, we can omit the clock skew from the right side of the inequality, allowing us to conclude that there is no hold-time violation.

(b) In this circuit, the shortest path from a flip flop output to a flip flop input contains 3 gate delays and since \(1 + 3 \times 0.3 < 1 + 1\), we would normally conclude that it is subject to internal hold time violations. However, this shortest path goes from the output of the bottom flip flop back to its input, and so we need not include the clock skew on the right side of the inequality, allowing us to conclude that there is no hold-time violation. All other feedback paths have at least 4 gate delays.

(c) In this circuit, the shortest path from a flip flop output to a flip flop input contains 3 gate delays and since \(1 + 3 \times 0.3 < 1 + 1\), we would normally conclude that it is subject to internal hold time violations. However, this shortest path goes from the output of the bottom flip flop back to its input, and so we need not include the clock skew on the right side of the inequality, allowing us to conclude that there is no hold-time violation. All other feedback paths have at least 4 gate delays and since \(1 + 4 \times 0.3 > 1 + 1\), these do not cause hold time violations.

(d) In this circuit, the shortest path from a flip flop output to a flip flop input contains 3 gate delays. There are two such paths that cause hold time violations, one from the output of the bottom flip flop, to the input of the middle flip flop (through the 3 input AND gate) and the other from the output of the middle flip flop to the input of the bottom flip flop (through the 4 input AND gate). Since \(1 + 3 \times 0.3 < 1 + 1\), both of these paths cause hold time violations. They can be corrected by adding an inverter pair at the inputs to the AND gates on the feedback paths. There is another path with 3 gate delays from the output of the middle flip flop to its input (through the 4 input AND gate), but this one does not cause a hold time violation. All other feedback paths have at least 4 gate delays and since \(1 + 4 \times 0.3 > 1 + 1\), these do not cause hold time violations.

5. For each of the circuits in Problem 1, determine the shortest clock period that can be used without causing any internal setup time violations. What maximum clock frequency does this correspond to? Assume that the flip flop setup time is 2 ns, the hold time is 1 ns, that gate delays for simple gates can range from .4 ns to 1.5 ns, that gates with 3 or 4 inputs have twice as much delay as simple gates, that the flip flop propagation delay can range from 1 ns to 4 ns and that the clock skew is 1 ns.

(a) Here the longest path from a flip flop output to a flip flop input has 2 gate delays, so the minimum period is \(4 + 2 \times 1.5 + 2 + 1 = 10\) ns, corresponding to a clock frequency of 100 MHz. In this case, we could actually neglect the 1 ns for clock skew, since there is just one flip flop. This would give 9 ns or 111 MHz.
(b) The longest path from a flip flop output to a flip flop input has 5 gate delays, so the minimum period is $4 + 5 \times 1.5 + 2 + 1 = 14.5 \text{ ns}$, corresponding to a clock frequency of 69 MHz.

(c) The longest path from a flip flop output to a flip flop input has 5 gate delays, so the minimum period is $4 + 5 \times 1.5 + 2 + 1 = 14.5 \text{ ns}$, corresponding to a clock frequency of 69 MHz.

(d) The longest path from a flip flop output to a flip flop input has 6 gate delays, so the minimum period is $4 + 6 \times 1.5 + 2 + 1 = 16 \text{ ns}$, corresponding to a clock frequency of 62.5 MHz.