Timing Issues in Digital Circuits

- Setup and hold time constraints
- Input timing constraints
- Clock period analysis
- Metastability and synchronizer reliability

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Edge-Triggered D Flip Flop

- D flip flop stores value at D input when clock rises
- Most widely used storage element for sequential circuits
- Propagation time is time from rising clock to output change
- If input changes when clock rises, new value is uncertain
  - output may oscillate or may remain at intermediate voltage (metastability)
- Timing rules to avoid metastability
  - D input must be stable for setup time before rising clock edge
  - must remain stable for hold time following rising clock edge
To avoid setup time violations, require

\[ \text{period} \geq (\text{max FF prop. delay}) + (\text{max comb. circuit delay}) + (\text{FF setup time}) + (\text{max clock skew}) \]

- CAD tools can check all FF-to-FF paths to verify
  - both component delays and wiring delays matter
  - accurate estimate requires component locations and information about routing of wires
Clock Period Analysis from Synthesis

Timing constraint: Default period analysis for Clock 'clk'
Clock period: 4.227ns (frequency: 236.560MHz)
Total number of paths / destination ports: 45 / 5

Delay: 4.227ns (Levels of Logic = 3)
Source: state_FFd1 (FF)
Destination: cnt_2 (FF)
Source Clock: clk rising
Destination Clock: clk rising

Data Path: state_FFd1 to cnt_2

<table>
<thead>
<tr>
<th>Cell:in-&gt;out</th>
<th>fanout</th>
<th>Delay (ns)</th>
<th>Delay (ns)</th>
<th>Logical Name (Net Name)</th>
</tr>
</thead>
<tbody>
<tr>
<td>FDR:C-&gt;q</td>
<td>9</td>
<td>0.626</td>
<td>1.125</td>
<td>state_FFd1 (state_FFd1)</td>
</tr>
<tr>
<td>LUT2:I1-&gt;O</td>
<td>1</td>
<td>0.479</td>
<td>0.740</td>
<td>_mux0001&lt;2-&gt;20_SW0 (N123)</td>
</tr>
<tr>
<td>LUT4:L:12-&gt;LO</td>
<td>1</td>
<td>0.479</td>
<td>0.123</td>
<td>_mux0001&lt;2-&gt;24_SW0 (N119)</td>
</tr>
<tr>
<td>LUT4:I3-&gt;O</td>
<td>1</td>
<td>0.479</td>
<td>0.000</td>
<td>_mux0001&lt;2-&gt;43 (_mux0001&lt;2&gt;)</td>
</tr>
<tr>
<td>FDS:D</td>
<td></td>
<td>0.176</td>
<td></td>
<td>cnt_2</td>
</tr>
</tbody>
</table>

Total Delay: 4.227ns (2.239ns logic, 1.988ns route)
(53.0% logic, 47.0% route)

synthesis estimates only; placement and routing information needed for accurate analysis
Hold Time Condition

- To avoid *internal* hold time violations, require
  \[
  \text{hold time} \leq (\text{min FF prop. delay})
  + (\text{min comb. circuit delay}) - (\text{max clock skew})
  \]
- CAD tools can check all FF-to-FF paths to verify
- In FGPAs, it is often the case that
  \[
  \text{hold time} < (\text{min FF prop. delay}) - (\text{max clock skew})
  \]
  so, hold time violations cannot occur
Timing Analysis of Sequential Comparator

- **Timing parameters**
  - gate delay: 0.25 to 1 ns
  - ff setup time: 2 ns
  - ff hold time: 1 ns
  - ff prop. delay: 0.5-2 ns
  - clock skew: 1 ns

- **Internal hold time violation?**
  - yes - 0.5 + 4(0.25) < 1 + 1
  - add inverter pair to feedback paths from ffs

- **Minimum clock period** - 2 + 6x1 + 2 + 1 = 11 ns or 90 MHz

- **Input timing requirements**
  - A and B must be stable from \((\text{clock\_edge} - 2) - 4\times1\) until \((\text{clock\_edge} + 1) - 3 \times 0.25\), so from -6 ns to +0.25

- **Output timing** - outputs can change 0.5 to 2 ns after clock
Reducing Clock Period

- Modify circuit to reduce max delays
- Replace ANDs, ORs with NORs
  - lower gate delays and eliminates feedback inverters
- Can sometimes adjust synthesis/implementation parameters to get better results from CAD tools
- More general methods
  - use low-delay circuit architectures
    - e.g. replace ripple-carry adder with carry lookahead
  - insert pipeline registers in large combinational logic paths
Combining Chip-Level Components

- When combining two components, may need to check setup constraints manually
  
  \[
  \text{clock period} \geq (\text{max output delay}) + (\text{max input delay}) + (\text{max inter-connect delay}) + \text{skew}
  \]

- Can check hold time violations using min input and output delays
  
  » hold time violations less likely across components, due to larger inherent delays, but possible if skew is also large
Input Delay Analysis from Synthesis

Timing constraint: Default OFFSET IN BEFORE for Clock ‘clk’
Total number of paths / destination ports: 17 / 12

Offset: 4.356ns (Levels of Logic = 4)
Source: \text{dIn (PAD)}
Destination: \text{cnt\_2 (FF)}
Destination Clock: \text{clk rising}

Data Path: \text{dIn} to \text{cnt\_2}

<table>
<thead>
<tr>
<th>Cell in-out</th>
<th>fanout</th>
<th>Gate Delay</th>
<th>Net Delay</th>
<th>Logical Name (Net Name)</th>
</tr>
</thead>
<tbody>
<tr>
<td>IBUF:1-&gt;O</td>
<td>7</td>
<td>0.715</td>
<td>1.201</td>
<td>d\text{in_BUF (dIn_BUF)}</td>
</tr>
<tr>
<td>LUT4:10-&gt;O</td>
<td>1</td>
<td>0.479</td>
<td>0.704</td>
<td>_mux0001&lt;2&gt;_map1</td>
</tr>
<tr>
<td>LUT4:13-&gt;LO</td>
<td>1</td>
<td>0.479</td>
<td>0.123</td>
<td>_mux0001&lt;2&gt;24_SW0 (N119)</td>
</tr>
<tr>
<td>LUT4:13-&gt;O</td>
<td>1</td>
<td>0.479</td>
<td>0.000</td>
<td>_mux0001&lt;2&gt;43_elps0&lt;2&gt;</td>
</tr>
<tr>
<td>FDS:O</td>
<td>0.176</td>
<td></td>
<td></td>
<td>cnt_2</td>
</tr>
</tbody>
</table>

\text{dIn} input should be stable, from 4.356 ns before clock edge, until clock edge.

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Total 4.356ns (2.328ns logic, 2.028ns route)
(53.4% logic, 46.6% route)
Summary of Timing Analysis

1. Check for internal hold time violations
   » for every ff-to-ff path, check
     
     \[(\text{minimum ff prop. delay}) + (\text{minimum comb. circuit delay}) \geq (\text{hold time}) + (\text{clock skew})\]
   » fix violations by adding delay
   » no violations possible if hold-time + skew < (min-ff-prop-delay)

2. Determine minimum clock period
   » find ff-to-ff path with largest value of
     
     \[(\text{maximum ff prop. delay}) + (\text{maximum comb. circuit delay}) + (\text{setup time}) + (\text{clock skew})\]
   » omit skew for paths from output to input of same ff

3. Input timing analysis
   » from each input, determine minimum delay from input to any flip flop in the circuit, and the maximum delay to any flip flop

4. Timing analysis for synchronous outputs
   » for each output, determine minimum delay from any flip flop to the output, and the maximum delay
   » include flip flop propagation delay and combinational circuit delay
How Input Delays Constrain Signals

- Component input signal changes are constrained by setup and hold times and input delays
  - stable period starts at clock – (setup + max delay)
  - and lasts until clock + hold – (min delay)
- Common simplification is to hold input stable from clock – (setup + max delay) until clock
Avoid Gated Clocks

- Two problems with right-hand circuit
  - Increases clock skew, making timing violations more likely
  - If load input goes high while clock is high, flip flop changes are not in sync with clock

- In general, best to avoid circuits that pass the clock signal through gates
  - In VHDL, avoid things like “if rising_edge(clk and X)”
Exercises

1. Consider the circuit shown below. The numbers labeling the paths are the minimum and maximum delays in picoseconds. Assume that the flip flop setup time is 200 ps, the hold time is 500 ps and the propagation delay is in the range [250,700] ps. Is this circuit subject to hold time violations? If so, explain how you would eliminate them? If not, how much larger would the hold time have to be in order to cause a hold-time violation. What is the minimum safe clock period for this circuit?

2. Suppose two copies of this circuit were connected together (that is, the output of one copy is connected to the input of another). What is the minimum safe clock period for the combined circuit?

3. Suppose that the clk goes high at time $t$. During what time period relative to $t$ must the inputs to the circuit in problem 1 be stable?
Metastability and Synchronizers

- Most digital systems have asynchronous inputs
  - keyboard input on a computer,
  - sensor on a traffic light controller,
  - card insertion on an ATM, etc.
- Asynchronous inputs change at unpredictable times
  - so, can change during clock transition, causing metastability
- Output of a metastable flip flop can oscillate or remain at intermediate value
  - leads to unpredictable behavior in other flip flops
  - metastability usually ends quickly, but no definite time limit
  - so, circuit failures due to metastability are unavoidable
  - however, systems can be designed to make failures rare
Synchronizers

- *Synchronizers* are used to isolate metastable signals until they are “probably safe”

- If the clock period is long enough, failure probability is small and expected time between failures is large.
  
  \[ MTBF = \text{Mean Time Between Failures} = (\alpha T/T_0)e^{T/\tau} \]
  
  where \( T \) is the clock period, \( \alpha \) is the average time between asynchronous input changes, \( \tau \) and \( T_0 \) are parameters of the flip flop being used.

- If \( T = 50 \text{ ns}, \alpha = 1 \text{ ms}, \tau = 1 \text{ ns}, T_0 = 1 \text{ ns}, \) MTBF \approx 8 \text{ trillion years}, if \( T = 10 \text{ ns}, \) MTBF becomes 220 seconds!
MTBF Chart

$\alpha T/T_0 = 100$ sec  1   .01   .0001

10 years
Variation on Basic Synchronizer

- Counter increases time for first flip flop to resolve if it becomes metastable
  - by increasing number of counter bits can make probability of synchronizer failure as small as we want (but not zero)
- But circuit, may fail to “see” some input changes
  - often there is a known minimum time between input changes, allowing all input changes to be observed
Exercises

1. Consider a synchronizer used to synchronize an asynchronous input signal. Let the flip flop parameters be $T_0 = 500 \text{ ps}$ and $\tau = 1 \text{ ns}$. If the clock period for the synchronizer is 10 ns, what is the probability that a single signal transition leads to a synchronizer failure? If the average time between changes of the input signal is 50 microseconds what is the mean time between synchronizer failures?

2. Given the parameters in problem 1, what is the smallest clock period (to the nearest ns) for which the mean time between failures is 100 years? What is the smallest clock period for which the mean time between failures is 10,000 years? Note: you may have to resort to trial-and-error calculations to solve this.

3. Given the parameters in problem 1, what is the largest value of $\tau$ that yields a mean time between failure of 100 years? What is the largest value that gives a mean time between failures of 10,000 years?

4. Consider problem 1 again. Suppose we know that the minimum time between changes to the input signal is 325 ns while the average is still 50 $\mu$s. Using the alternate synchronizer design on slide 16, how big can the counter be and still guarantee that no input signal transitions are missed? What is the mean time between failures if this counter length is used? Assume that the clock period is 10 ns.