1. Prove that the gates shown below are equivalent.

2. Draw a circuit diagram of a CMOS implementation of a three input NOR gate.
3. Draw a circuit that implements a two input multiplexor using only NAND gates and inverters. What is the worst-case propagation delay through this circuit, if an inverter has a worst-case delay of 100 ps and a NAND gate has a worst-case delay of 200 ps?