Please print out this form (two-sided, if you can) and write your answers legibly in the spaces provided. If you can’t write legibly, type.

1. Explain how to modify the VHDL for the 4-way max-finder, so that the three 2-way max-finders are all Moore-mode state machines. How does this affect the interface timing diagram for the 4-way max-finder?

2. Show how to modify the binary input module so that the pulse signals are generated when the buttons are released.
3. In the binary output module, if the counter were ten bits long, how often would the update signal go high? Assume the circuit is implemented on the prototype boards.