Please print out this form (two-sided, if you can) and write your answers legibly in the spaces provided. If you can’t write legibly, type.

1. Is the pulse counter a Mealy mode sequential circuit? Explain.

2. Explain why the VHDL implementation of the debouncer does not require a state signal?
3. The knob interface described in the text has a *tick* output and a *clockwise* output. We could have defined the knob interface with two different outputs, *upTick* and *downTick*, where *

*upTick* = 1 for one clock tick, when the knob turns in the clockwise direction and *

*downTick* = 1 for one clock tick, when knob turns in the counter-clockwise direction. Rewrite the VHDL spec to use this interface instead of the original.