1. Given the declarations
   
   ```vhd
   type shape is (square, rectangle, trapezoid, triangle, pentagon);
   subtype quadrilateral is shape range square to trapezoid;
   signal s1, s2: shape;
   signal q1, q2: quadrilateral;
   ```

   which of the following assignments are allowed.
   
   ```vhd
   s1 <= square; s2 <= q1; q2 <= s2; q1 <= s1; q1 <= pentagon;
   ```

2. Is the type `std_logic` a built-in type of the VHDL language? How many possible distinct values can a signal of type `std_logic` take on?
3. In the process shown below, which assignments are synchronous and which are asynchronous? Why?

```vhdl
process (clk, t, x) begin
  if rising_edge(clk) then
    t <= s;
    if en = '0' then
      s <= '0'; t <= '1';
    else
      s <= x xor s;
    end if;
  end if;
  y <= t and x;
end process;
```