Please print out this form (two-sided, if you can) and write your answers *legibly* in the spaces provided. If you can't write legibly, type.

1. Consider the declaration
   ```vhdl
   signal x: std_logic_vector(0 to 7);
   ```
   what are the values of the following attributes
   
   `x'low`  `x'right`  `x'range`  `x'length`

2. Write a VHDL function `slv(i,length)` that converts an integer `i` to a
   
   `std_logic_vector` with the specified length and index range `length–1 downto 0`
   
   You may use the conversion functions defined by the IEEE library to help with this.
3. Rewrite the following VHDL process without using variables. You will need to unroll the loop. Assume \( a \) and \( z \) are unsigned signals with index range (2 downto 0).

```vhdl
process (clk)
variable x : unsigned(2 downto 0);
variable y : std_logic;
begin
  if rising_edge(clk) then
    x := "001";
    y := '0';
    z <= a + "001";
    for i in 0 to 3 loop
      if y = '1' then z(i) <= x(i); end if;
      y := y xor z(i);
      x := x + "001";
    end loop;
  end if;
end process;
```