As part of this course you will design, implement in VHDL, and test a pipelined processor. In this assignment, you will develop: your processor specification, sample programs, your pipeline design, and a project timeline. This project will be completed in groups of three students. Please note that your final project report will require all of the information requested below, so you are advised to structure your materials to make it easy to integrate them together at the end of the semester.

1. **Project Group Formation**

Finalize your group (initial group assignments were given in class) and choose a name for your processor. Submit a status report no later than Monday, October 12 listing your group members and processor name. Send this status report to Prof. Crowley and the TA via email with the following subject text: “560: Project group and name”. Include this information in your hard-copy, in-class submission on October 19.

2. **Modified MIPS Machine Requirements**

Your task is to develop a MIPS-style processor with the following properties:

- 32-bit instructions
- A useful subset of MIPS instructions, no fewer than 16. Feel free to add instructions not found in the MIPS ISA.
- A useful subset of the MIPS addressing modes
- Support for integer operations
- A pipeline with five stages
- Hardware support for two thread contexts, supporting either a fine- or coarse-grained scheduling discipline
- Register files with 32, 32-bit registers (you are free to define additional special purpose registers, e.g., HI and LO registers for mult/div results)

Specify the machine instruction set (both the assembly language mnemonics and machine instruction encoding), and addressing modes.

3. **Test Programs**

**Program 1: sort.** Write a simple sorting program in your machine’s assembly language. The program should sort an array of 32 integers into descending order. You should also write and submit the assembly program that loads the array into memory.
**Program 2: stats.** Write an assembly language program that finds the average, maximum and minimum value of the array of 32 integers. The program should also record the array addresses that hold the maximum and minimum values.

4. **Processor Pipeline Design**

Before you begin modeling your processor, you must design it! For this project milestone, you must:

- Design the five stage pipeline for the dual threaded processor.
- Draw a picture of the processor pipeline indicating each stage. This should be similar in style to Figure A.18 in H&P. Each stage should have a name.
- Indicate the actions associated with each stage. This should have two parts.
  - A text description of what happens in each stage.
  - A formal description similar to Figure A.19 in H&P.
- Describe the hazards that are possible in your design, and how they are to be handled.

Hand these materials in as part of the write-up for this milestone (and remember to structure them to be easily included in the final report).

5. **Project Plan**

In this final component of the milestone, the ultimate objective is to generate a project timeline and to assign group member responsibilities in order to ensure a balanced team effort and a timely project completion. To do this, you will need to think in detail about what tasks are required between now (i.e., after the machine specification) and the completion of your tested processor design.

Write out a structured list of design, implementation, and debugging tasks that will be required to finish this project. Also provide a list of questions and issues that your group needs to resolve before starting on the detailed design (you may have many questions at this point). Using these structured lists, provide a timeline for project completion and an assignment of responsibilities to group members. The final project presentation and demonstration will happen on November 23rd. Additionally, your group’s final report will be due at the start of the final scheduled class meeting time, 4:00PM on December 7th.