Computer Systems Organization

CSE 521/560M
Lecture 7
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Plan for Today

- Questions
- Clock discussion
- Conclude L6
Sample Clock Module

-- This file contains the code to generate a
-- clock. The clock output begins with 0.

entity clock is
  port (period : in time;
          clock_value : out bit);
end clock;

architecture clock_tick of clock is
begin
  -- The clock value should change
  -- every half of the period.
  clock_generate: process is
    constant wait_time : time := period / 2;
    begin
      clock_value <= '0';
      wait for wait_time;

      clock_value <= '1';
      wait for wait_time;

    end process clockGenerate;
end clock_tick;

Assignment

- Readings
  - For Wednesday
    - H&P: 3.5-3.6
    - Ash: Chapter 6
  - For Monday
    - H&P: 3.7-3.9
    - Ash: Read Chapter 7
Conclude L6