Computer Systems Organization

Homework #2

Due: Wednesday, October 29
(with a status report required on Friday, October 17)

As part of this course you will design, implement in VHDL, and test a pipelined processor. In this assignment, you will develop: your processor specification, sample programs, and a project timeline. This project will be completed in groups of up to three students.

1. Project Group Formation

Establish your group and choose a name for your processor. Submit a status report no later than Friday, October 17 listing your group members and processor name. Include this information in your homework submission on October 29.

2. Modified MIPS Machine

Your task is to develop a MIPS-style processor with the following properties:

- Two instruction word lengths: 16- and 32-bits
- No more than 12 instructions for each length
- A useful subset of the MIPS addressing modes
- Support for integer operations
- A pipeline with three stages
- Hardware support for two thread contexts
- Register files with 32, 32-bit registers (you are free to define additional special purpose registers, e.g., HI and LO registers for mult/div results)

Specify the machine instruction set (both the assembly language mnemonics and machine instruction encoding), addressing modes, and pipeline stages and operation.

3. Programs

Program 1: sort. Write a simple sorting program in your machine’s assembly language. The program should sort an array of 32 integers into descending order. You should also write and submit the assembly program that loads the array into memory.

Program 2: stats. Write an assembly language program that finds the average, maximum and minimum value of the array of 32 integers. The program should also record the array addresses that hold the maximum and minimum values.

4. Project Plan
In this final component of the homework, the ultimate objective is to generate a project timeline and to assign group member responsibilities in order to ensure a timely project completion. To do this, you will need to think in detail about what tasks are required between now (i.e., after the machine specification) and the completion of your tested processor design.

Write out a structured list of design, implementation, and debugging tasks that will be required to finish this project. Also provide a list of questions and issues that your group needs to resolve before starting on the detailed design. Using these structured lists, provide a timeline for project completion and an assignment of responsibilities to group members. The overall project report and presentation will happen during the last week of class. Additionally, your group will demonstrate the operation of the VHDL model to Prof. Crowley outside of class (either during the last week of class or during finals week).